AURIX Analog-to-Digital Converters
Introduction to ADC

ADC Theory
- Sampling
- Resolution
- Nonlinearities
- Dynamic range
- SAR ADC example

AURIX ADC
- AURIX ADC Modules
- EVADC Groups & Channels
- EVADC Conversion Queue
- EVADC Initialisation Sequence

Hands-on session
Introduction to ADC

ADC is a circuit that converts an analog signal (voltage variation over time) into discrete form (digital values) that can be processed by HW or SW

Types of ADC:
- **SAR** – Successive Approximation Register ADC
- **DSADC** – Delta-Sigma (Sigma-Delta) ADC
- **FLASH-ADC**
- Pipeline ADC
- Dual-Slope
ADC characteristics

**Key Characteristics**
- Sampling Rate
- Resolution
- DC & AC nonlinearities
- Dynamic range
- Supply level, consumption
- Input types
- Output format
The **sample rate** or sampling frequency is the maximum rate at which an ADC can convert the analog signal into a digital data.

The selection of the Sampling rate depends on the input signal's highest frequency component (fa) and is defined by the **Nyquist frequency** (fs):

\[ fs \geq fa \times 2 \]

Understanding the input signals properties e.g. highest frequency content is an important part of getting accurate measurements and avoiding Aliasing.
The resolution determines the minimum change in the input signal that makes the output change by one count.

The resolution is expressed as a number of output bits. The smallest increment in the signal value that can be recognized by an ADC is defined as least significant bit (LSB):

\[ 1 \text{ LSB} = \frac{V_{\text{ref}}}{2^N - 1} \]

<table>
<thead>
<tr>
<th>Resolution, N</th>
<th>(2^N)</th>
<th>LSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>8bit</td>
<td>255</td>
<td>10 mV</td>
</tr>
<tr>
<td>10bit</td>
<td>1024</td>
<td>5 mV</td>
</tr>
<tr>
<td>12bit</td>
<td>4096</td>
<td>1.22 mV</td>
</tr>
<tr>
<td>14bit</td>
<td>16384</td>
<td>0.3 mV</td>
</tr>
<tr>
<td>16bit</td>
<td>65536</td>
<td>0.075 mV</td>
</tr>
</tbody>
</table>

V_{\text{ref}} = 5V
ADC Nonlinearities

Transfer function nonlinearities in a real ADC

Total Unadjusted Error (TUE) defines the maximum deviation (in LSBs) from the ideal transfer curve

\[ TUE = \sqrt{\text{Offset}^2 + \text{Gain}^2 + \text{DNL}^2 + \text{INL}^2} \]
Dynamic range defines the ratio between the minimum and the maximum input values that an ADC can reliably convert.

The achieve maximum conversion precision the input signal has to match to the dynamic range of an ADC. The signal amplification or attenuation might be required.

Data Conversion

\[ \text{Digital\_value} = \frac{\text{Vin}}{\text{Vref}} \times (2^N - 1) \]

\[ \text{Vin} = \frac{\text{Digital\_value}}{\left(\frac{2^N}{2^N - 1}\right)} \times \text{Vref} \]
SAR ADC

This sampled input from Sample & Hold (SH) capacitor is fed into a comparator along with the input from an internal DAC, the output of which is adjusted in binary increments to get as close as possible to the sampled value.

SAR ADC employs a binary search algorithm to match an input voltage with a reference value.

4-bit conversion example
AURIX TC3x ADC

Three ADC types in AURIX

- **SAR** x 12 by 8/16 channels
  - **EVADC** Primary 12 bit, ≤ 2.5MS/s
  - **EVADC** Secondary 12 bit, ≤ 1.4MS/s
- **Fast Compare** x8 10 bit, ≤ 5MS/s
- **EDSADC** x14 16 bit, ≤ 200KS/s

TC375: 8 x EVADC, 4 x FCC, 6 x EDSADC
EVADC Group & Channels

Each **EVADC Group** is an independent SAR converter that consists of 8 (or 16) input channels, Multiplexer, Converter, Control Logic, Request control and Result handling.

EVADC input channels are multiplexed to connect the corresponding signal source to the converter one at a time. For each channel, the sample time can be controlled individually.
**EVADC Conversion**

EVADC is designed to execute complex sequences of conversions by filling up *Queues*

### Conversion Request
Conversion sequence can be started (requested) by 3 different sources:
- Software Trigger
- Self-Timed Trigger,
- External Trigger e.g. GPIO, GTM

The requested conversion can be executed once or repeatedly after trigger.

### Arbiter
When multiple conversion requests are used arbitration process defines which conversion is executed next based on assigned priorities.
Enable a primary/secondary group and prepare it for operation

**EVADC_GxANCFG = 0x00300000**
; Analog clock frequency is 160 MHz / 4 = 40 MHz (example)
; CALSTC = 0

**EVADC_GxAARB_CFG = 0x0000003**
; Enable analog block

**WAIT**
; Pause for extended wakeup time (≈ 5 µs)

**EVADC_GLOBCFG = 0x80000000**
; Begin start-up calibration
; (other operations can be executed in the meantime)

**EVADC_GxAARBPR = 0x01000000**
; Enable arbitration slot 0

**EVADC_GxQMR0 = 0x00000001**
; Enable request source 0

**EVADC_GxICLASS0 = 0x00000002**
; Select 4 clocks for sampletime 4 / 40 MHz = 100 ns
; The default setting stores results in GXRES0,
; service requests are issued on GxSR0

**EVADC_GxRCR0 = 0x80000000**
; Enable result service requests, if required

**EVADC_GxQINR0 = 0x00000020**
; Request channel 0 in auto-repeat mode

**WAIT**
; Wait for start-up calibration to complete
; (other operations can be executed in the meantime)
; ---> This starts continuous conversion of the channel

### EVADC basic setup sequence

- **Clk & Analog Block enable**
- **Request source and queue settings**
- **Sample time settings**
- **Start conversion**
- **Wait for the 1st conversion result**
ADC_Single_Channel_1 for KIT_AURIX_TC375_LK

Code Example

```
STM32 HAL ADC

// 1. Define interrupt service routine.
2  STM32F4 HAL ADC
3  STM32F4 HAL ADC
4  STM32F4 HAL ADC
5  STM32F4 HAL ADC
6  STM32F4 HAL ADC
7  STM32F4 HAL ADC
8  STM32F4 HAL ADC
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197  STM32F4 HAL ADC
198  STM32F4 HAL ADC
199  STM32F4 HAL ADC
200  STM32F4 HAL ADC
```

Tutorial

ADC_Single_Channel_1 for KIT_AURIX_TC375_LK
ADC single channel conversion
Resources

Books


Application Notes

AP56003 A Guide to the Analog Part of the A/D Converter

AP32297 A/D Converter Supply and PCB Design Guideline

Code examples & Tutorials

https://github.com/Infineon/AURIX_code_examples/blob/master/code_examples

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