**MOSFET PARAMETERS FOR HAND CALCULATION**

<p>| | | | | | |</p>
<table>
<thead>
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<tr>
<td>nMOSFET</td>
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<td>1.1 \times 10^{-7}</td>
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<td>11.2</td>
<td>0.32</td>
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<td>pMOSFET</td>
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<td>1.5 \times 10^{-7}</td>
<td>0.2</td>
<td>11.2</td>
<td>0.32</td>
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(*) You may use the approximate relation: \( C_{IS} \approx C_{GS} W_0 \), \( C_{DS} \approx C_{GD} W_0 \)

**PROBLEM 1**

Consider the common source (CS) amplifier shown in the figure below, where the supply voltage \( V_{DD} = 1.2 \, \text{V} \), the source resistance \( R_S = 10 \, \text{k}\Omega \) and the load capacitance \( C_L = 10 \, \text{ff} \). Then:

1) determine the device channel length \( L \) so that the transconductance efficiency \( g_m I_D = 10 \) and the intrinsic gain \( a_0 = 22 \);
2) determine the device channel width \( W \) so that \( C_{GS} = 15 \, \text{ff} \);
3) determine the value of \( R_S \) so that \( V_{DS} = V_{GD} / 2 \);
4) derive the expression of the frequency response of the circuit and trace its Bode plot;
5) considering only the dominant pole of the frequency response, derive the expression and the value of the frequency where the amplitude of the frequency response is equal to 1.

**SOLUTION**

1) MOSFET channel length \( L \)

\[
\frac{g_m}{I_D} = \frac{2}{V_{DS}} = 10 \quad \Rightarrow \quad V_{DS} = 0.2 \, \text{V}
\]

\[
a_o = \frac{g_m R_S}{V_{DS}} = 2 \frac{I_D}{V_{DS}} \cdot \frac{M_L}{I_D} = L = \frac{g_m}{a_0} \quad \frac{V_{DS}}{M_L} = 200 \, \mu\text{m}
\]

2) MOSFET channel width \( W \)

\[
C_{GS} = \frac{2}{3} \frac{C_{xW}}{W} + C_{xsoW} = 15 \, \text{fF} \quad \Rightarrow \quad W = \frac{C_{gs}}{2/3 \frac{C_{xW}}{W} + C_{xso}} = 8.2 \, \mu\text{m}
\]

3) \( R_S \) so that \( V_{DS} = V_{DD} / 2 \)

\[
V_{DS} = V_{DD} - R_S I_D \quad I_D = \frac{1}{2} \frac{k_n}{L} V_{DS}^2 \quad V_{DS} = 38.9 \, \mu\text{A}
\]

\[
R_S = \frac{V_{DD} - V_{DS}}{I_D} = \frac{V_{DD} - V_{DS}}{2I_D} = 1.59 \, \text{k}\Omega
\]

4) Frequency response \( Av(f_w) = \frac{V_O}{V_S} \)

Small-signal equivalent circuit
\[ A_v(j\omega) = \frac{V_o}{V_i} = -\frac{g_m R_o (1 - j\omega C_d/g_m)}{1 + j\omega R_o C_o} \]

\[ R_o = R_e \parallel R_d \]

\[ Y_i = \frac{i_i}{V_i} = \frac{j\omega C_s + j\omega C_d (1 + g_m R_o)}{A + R_s Y_i} \]

\[ Y_i = \frac{2}{\omega + A_s} \quad V_o = \frac{V_s}{A + R_s Y_i} = \frac{V_s}{A + j\omega R_s C_i} \quad C_i = C_d + C_d (1 + g_m R_o) \]

\[ A_v(j\omega) = \frac{V_o}{V_s} = \frac{V_o}{V_i} \frac{V_i}{V_s} = -A_v \frac{1 - j\omega/w_2}{(1 + j\omega/w_{p1}) (1 + j\omega/w_{p2})} \]

\[ A_v = g_m R_o = 4.71 \]

\[ \omega_s = 2\pi f_s = \frac{g_m}{C_d} = 2\pi \cdot (234 \text{ GHz}) > \omega_r \text{ irrelevant} \]

\[ \omega_{p1} = 2\pi f_{p1} = \frac{1}{R_s C_i} = 2\pi \cdot (528 \text{ MHz}) \text{ dominant pole} \]

\[ \omega_{p2} = 2\pi f_{p2} = \frac{1}{R_o C_o} = 2\pi \cdot (8.02 \text{ GHz}) \text{ non-dominant pole} \]

\[ |A_v(j\omega)| \text{ dB} \]

\[ -20 \text{ dB/dec} \]

5) Unity-gain frequency of the dominant-pole frequency response
Assuming \[ A_v(j\omega) = -\frac{A_v}{1 + j\omega/\omega_p} \]

Then \[ |A_v(j\omega_0)| = 1 \Rightarrow \frac{A_v}{\sqrt{1 + (\omega_0/\omega_p)^2}} = 1 \]

\[ \omega_0 = \omega_p \sqrt{A_v^2 - 1} = 2.4\, \text{kHz} \]

If we remove the dominant-pole behavior assumption, then:

\[ u_0 = A_v \sqrt{\frac{1 + (\omega_0/\omega_p)^2}{1 + (\omega_0/\omega_p)^2}} = 1 \]

\[ \frac{\omega_0^2}{\omega_p^2} + \omega_0^2 \left( \frac{1}{\omega_p^2} + \frac{1}{U_i^2} - \frac{A_v^2}{\omega_p^2} \right) + 1 - \frac{A_v^2}{\omega_p^2} = 0 \]

\[ \omega_0 = 2.33\, \text{GHz} \]

**Problem 2**

Consider the circuit shown in the figure below, where the supply voltage \( V_{DD} = 1.2\, \text{V} \), the bias current \( I_b = 1\, \text{mA} \), the signal source \( I_s \) generates a sinusoidal current with frequency large enough for capacitor \( C \) to be considered an ac short circuit. Using the MOSFET parameters at the top of the previous page and the data below:

1) determine the device gate width \( W \) so that the transconductance \( g_m = 10\, \text{mS} \);
2) determine the value of \( V_D \) so that the dc component of the input voltage \( V_I = 0.2\, \text{V} \);
3) derive an analytic expression for the transfer function \( A(s) = I_D/I_i \) (current gain).

**Data**

\( V_T = 0.4\, \text{V} \), \( L = 120\, \text{nm} \); \( R_D = 0.5\, \text{k} \); \( R_I = 5\, \text{k} \).

**Solution**

1) **Device gate width \( W \)**

\[ I_D = I_b \quad g_m = \sqrt{2kT/W} \quad I_D = 10\, \text{mS} \quad \Rightarrow \quad W = L \cdot \frac{g_m^2}{2kT} \quad W = 12.8\, \mu\text{m} \]

2) **Gate voltage \( V_G \)**

\[ V_G = V_I + V_{GS} = V_I + V_{RW} + V_{OV} = 0.8\, \text{V} \]

\[ V_{OV} = \frac{2I_D}{g_m} = 0.2\, \text{V} \]

Note: we are neglecting the body effect.
that would increase $V_{TH}$ value

3) Current gain $A_i(s) = \frac{i_o}{i_i}$

\[
\Phi I_B = \text{const} \Rightarrow \text{ac open}
\]

KCL at output node:
\[
v_o \left( \frac{1}{R_D} + \frac{1}{R_o} + sC_o \right) - v_i \left( \frac{1}{sC_s} + \frac{1}{R_d} \right) = 0
\]

\[
R_o = \frac{\mu_m L}{I_D} = 1.32 \ \mu \Omega \Rightarrow \ \beta_0 = \frac{1}{R_o} = 758 \ \mu S \ll \ \beta_m = \beta_m (1 + x) = 12 \ \text{mS}
\]

\[
v_o = \frac{\beta_m R_D}{1 + s R_D \alpha} \cdot v_i, \quad R_0 = R_0 || R_D
\]

\[
i_i = V_i \cdot \frac{1}{R_D} \left( s C_i + \beta_m + \frac{1}{R_o} \right) v_i - \frac{1}{R_o} v_o =
\]

\[
= \left( s C_i + \beta_m + \frac{1}{R_o} - \frac{\beta_m R_D}{1 + s \alpha} \right) v_i, \quad \alpha = \frac{1}{\beta_m C_0}
\]

\[
= \beta_m \left( \frac{s^2 C_i + \beta_m + s \beta_m}{s^2 C_i + \beta_m + \frac{R_o}{R_o + R_D}} \right) v_i
\]

\[
= \beta_m \left[ \frac{1 + s (z + \beta_m)}{1 + s C} \right] v_i, \quad z = \frac{1}{R_o C_0}
\]

\[
\frac{\beta_m}{C_i} = 2\pi \cdot (89.8 \ \text{GHz}), \quad \frac{1}{C} = 2\pi \cdot (44.6 \ \text{GHz})
\]

MOSFET transit frequency: $\omega_T = \frac{\beta_m}{C_i + C_d} = 2\pi \cdot (81.1 \ \text{GHz})$

Taking into account that the maximum operating frequency of the circuit in practice is going to be $\ll \omega_T$, the
\[ Y_i = \frac{A_i V_i}{V_i} = \frac{\text{gm} I_i}{R_s + R_D} \]

\[ I_i = \frac{A_i}{R_s} \frac{V_i}{R_s + 2i} = \frac{I_s}{R_s} \frac{V_i}{V_i + 1} = \frac{\text{gm} R_s}{R_s + 1} \]

\[ A_i(s) = \frac{V_o}{I_s} = -\frac{\text{gm}}{R_s + 1} \frac{1}{V_i} \frac{I_s}{I_s + R_D} \]

\[ = -\frac{\text{gm} R_s}{1 + \frac{R_s R_D}{R_D}} \cdot \frac{1}{V_i} \]

\[ = -\frac{R_s}{1 + \frac{R_D}{R_D}} \cdot \frac{\text{gm} R_s}{1 + \frac{R_D}{R_D}} \]

**Problem 3**

Consider the two circuits shown in the figure below, and discuss the advantages in terms of frequency response \(A_i(s) = \frac{V_o}{I_i}\) of topology (b) with respect to topology (a) when the internal parasitic capacitances of the two MOSFETs are negligible with respect to the load capacitance \(C_L\).

Using the MOSFET parameters at the top of the previous page and the data below, determine the low-frequency gain and the frequency of the dominant pole in the two cases.

**Data**

\( V_{\text{IN}} = 0.4 \, \text{V}, \, I_{\text{B1}} = 100 \, \mu\text{A}, \, g_{\text{m1}}/I_{\text{B1}} = 15, \, R_D = 4 \, \text{k}\Omega, \, L_1 = 240 \, \text{nm}, \, L_2 = 120 \, \text{nm}, \)

\( I_e = 2 \, \text{mA}, \, V_{\text{OV2}} = 0.2 \, \text{V}, \, C_L = 200 \, \text{fF}. \)

**Solution**

In topology (a), the large capacitive load \(C_L\) is driven directly by the common-source stage, whose frequency response \(A_i(s) = \frac{V_o}{I_i}\) features a dominant pole at,

\[ f_{cs} = \frac{1}{2\pi R_0} \frac{1}{C_0} \quad R_0 = R_{\text{OL}} R_D \quad C_0 = C_L + C_{\text{DS1}} \]

In topology (b), the CS stage drives the much smaller input capacitance of the common-drain stage, \(C_{sc} < C_{\text{DS1}} + C_{\text{GS2}}\), which moves the CS dominant pole at higher frequencies:

\[ f_{cs} = \frac{1}{2\pi} \frac{1}{R_0 \left(C_{\text{DS1}} + C_{\text{GS2}} + C_{\text{GS2}}\right)} \ll C_L \]

The CD stage introduces an additional pole at

\[ f_{cb} = \frac{1}{2\pi} \frac{g_{\text{m}}}{C_{\text{GS2}} + C_{\text{DS2}} + C_L} \approx \frac{1}{2\pi \frac{g_{\text{m}}}{C_L}} \quad f_{cb} \ll f_{cs} \quad \Rightarrow \quad f_D \approx \frac{1}{2\pi R_0 C_L} \]
dc analysis

\[ g_{m1} = \frac{g_m}{I_{D1}} \quad I_{D1} = (15 \text{ V}^{-1}) (100 \text{ mA}) = 1.5 \text{ mS} \quad R_{o1} = \frac{V_{m}}{I_{D1}} = 26.4 \text{ k}\Omega \]

\[ W_1 = L_1 \quad \frac{g_{m1}}{2K_mI_{D1}} = 5.75 \mu \text{m} \]

\[ g_{m2} = \frac{2I_{D2}}{V_{O2}} = \frac{2I_{D2}}{V_{O2}} = 20 \text{ mS} \quad R_{o2} = \frac{V_{m}L_2}{I_{D2}} = 660 \Omega \]

\[ W_2 = L_2 \quad \frac{g_{m2}}{K_mV_{O2}} = 25.5 \mu \text{m} \]

Low-frequency gain

(a) \[ A_{vo} = -g_{m1} \frac{r_{o1} \| R_D}{-5.21} \]

(b) \[ A_{vo} = \frac{V_o}{V_i} = \frac{V_o}{V_{i2}} \frac{V_{i2}}{V_i} = \left( \frac{g_{m2}}{g_{m1} + \frac{1}{r_{o2}}} \right) \left( -g_{m1} \frac{r_{o1} \| R_D} \right) = -4.08 \]

Dominant pole

(a) \[ \frac{1}{C_{B1}} \]

single pole at

\[ f_c = \frac{1}{2\pi R_o(C_{B1} + C_{B2} + C_L)} = 224 \text{ MHz} \]

\[ R_0 = r_{o1} \| R_D \]

(b) common-drain stage

\[ C_{B2} \]
Pole frequency
\[ f_{CD} = \frac{g_m V_i + V_{il}}{C_{ds2} + C_{ds1} + C_L} = 15.7 \text{ GHz} \]

Input capacitance
\[ C_{CD} = C_{ds2} + g_{m2} \left( 1 - \frac{V_o}{V_{il}} \right) = C_{ds2} + g_{m2} \left( 1 - \frac{g_{m2}}{g_{m1} + V_{il}} \right) \]
\[ \text{Miller's theorem} \]
\[ = 14.8 \text{ fF} \]

CS stage
\[ f_{CS} = \frac{1}{2 \pi R_C (C_{ds1} + C_{gs1} + C_{CD})} = 2.37 \text{ GHz} < f_{CD} \]

Dominant pole
\[ f_{CS} = 2.37 \text{ GHz} \Rightarrow f_{CS} = 224 \text{ MHz} \]
\[ CS < CD \quad \text{CS above} \]