Basic building block for analog ICs:

- enables differential signal processing
- increased immunity to noise and disturbances
- 2x twice the maximum signal amplitude with respect to unipolar signal proc.

- requires good matching between devices

**Assumptions:**
- $n_1$ and $n_2$ are identical
- $I_B$ (bias or tail current) constant ($=\text{indep. of } V_S$)

**Input and output signals:**
- differential input: $V_{ID}(t) = V_{I1}(t) - V_{I2}(t)$
- $V_{ID}$ is transformed into a change of $I_{01}$ and $I_{02}$
- the impedance of the active load transforms the current variation into a voltage variation
- differential or single-ended (unipolar) output voltage depending on the active load

*Large-signal analysis of the DP*
Large-signal analysis of the DP

\[ V_{i1} - V_{i2} \]

\[ I_01, I_02 \]

Assume \( n_1, n_2 \) in saturation.

Define:

\[ V_{iD} = V_{i1} - V_{i2} \]  differential comp.
\[ V_{DC} = \frac{V_{i1} + V_{i2}}{2} \]  common-mode component

Then:

\[ V_{i1} = V_{DC} + V_{iD}/2 \]
\[ V_{i2} = V_{DC} - V_{iD}/2 \]

KCL at the common source node of \( n_1 \) and \( n_2 \)

\[ I_{o1} + I_{o2} = I_B \Rightarrow 0 \leq I_{o1}, I_{o2} \leq I_B \]

Balanced (equilibrium)

\[
\begin{align*}
 V_{o11} &= V_{o21} &= \sqrt{\frac{2I_B}{k_{n1} W/L}} &= \sqrt{\frac{2I_B}{k_{n1} W/L}} \\
 V_{o12} &= V_{o22} &= \sqrt{\frac{I_B}{k_{n1} W/L}} \\
 & & & \text{valid when } V_{iD} = 0
\end{align*}
\]

If \( V_{iD} > 0 \) \( \Rightarrow V_{CS1} > V_{CS2} \Rightarrow I_{o1} > I_{o2} \)

Define: \( V_{iDh} \) : value of the differential input voltage \( V_{iD} \) when \( I_{o1} \) becomes equal to \( I_B \) and \( I_{o2} = 0 \)

\[
\begin{align*}
 I_{o1} &= \frac{k_{n1}}{2} \frac{W}{L} (V_{i1} - V_S - V_{IN})^2 = I_B \Rightarrow (V_{i1} - V_S - V_{IN})^2 = \frac{2I_B}{k_{n1} W/L} \\
 I_{o2} &= \frac{k_{n1}}{2} \frac{W}{L} (V_{i2} - V_S - V_{IN})^2 = 0 \Rightarrow (V_{i2} - V_S - V_{IN})^2 = 0
\end{align*}
\]
\[ V_{102} = \frac{k_{m}}{2} \frac{V_{g}}{L} \left( V_{T_2} - V_{5} - V_{1n} \right)^2 = 0 \Rightarrow \left( V_{T_2} - V_{5} \right) = V_{1n} \]

\[ V_{T_1} - V_{T_2} = \sqrt{\frac{2 I_B}{k_{m} L}} = \sqrt{2} V_{0v} = V_{10h} \]

What if \( V_{ID} < 0 \) = anti-symmetrical

\[ i_{T_2} > i_{T_1} \text{ up to the point where } i_{T_2} = I_B \]

and \( i_{T_1} = 0 \) : \( V_{ID} = V_{10L} = - V_{10h} = - \sqrt{2} V_{0v} \)

What if \( V_{IC} \) changes?

Assume: \( \Delta V_{IC} > 0 \)

\[ \Delta V_{IC} \uparrow \quad \Delta V_{Q1} = \Delta V_{Q2} = \Delta V_{IC} - \Delta V_{S} \]

\[ \Rightarrow \Delta i_{T_1} = \Delta i_{T_2} \]

Since \( i_{T_1} + i_{T_2} = I_B \)

\[ \Rightarrow \Delta V_{Q1} = \Delta V_{Q2} = \Delta V_{S} = \Delta V_{IC} \]

provided that

\[ I_B = \text{const.} \]

**Small-signal analysis of the DP**

Since we are dealing with a LINEAR equivalent circuit we can split the analysis into two parts:

- differential-mode analysis: \( V_{IC} = 0 \), \( V_{ID} \neq 0 \)
- common-mode analysis: \( V_{IC} \neq 0 \), \( V_{ID} = 0 \)

In both cases we assume that the DP is balanced in dc
\[ V_{id} = 0 \]

Differential-mode analysis:
\[ v_{ic} = 0, \quad v_{id} 
eq 0 \]
\[ v_{i4} = V_{id}/2 \]
\[ v_{i2} = -V_{id}/2 \]

\( V_s = 0 \) due to circuit symmetry and to the anti-symmetric input

Half circuit:
\[ V_{id} \]
\[ v_{id}/2 \]
\[ I_{ac, ground \ s} \]
\[ v_s = 0 \]

The other half is exactly the same circuit but with an opposite input \( \Rightarrow \) opposite output \( I_{o2} = -I_{o1} \)

Common-mode analysis:
\[ v_{ic} \neq 0, \quad v_{id} = 0 \]
\[ V_{i4} = V_{i2} = v_{ic} \]

\[ I_B = I_{b3} = N \cdot I_{ref} \]
\[ W_3 = N \cdot W_4 \]
ac ground since $V_{G3} = \text{const.}$

Left half: $V_{IC} \rightarrow \Rightarrow \quad i_{o2} = i_{o1}$

At low frequency

\[ V_{IC} = V_{GS1} + V_{GS1} \]

\[ V_{GS1} = V_{IC} - V_S \]

\[ V_{GS1} = V_S \]

\[ V_{IC} \]

\[ \text{ac short circuit} \]

\[ R_01 \]

\[ 2R_03 \]

\[ + \]

\[ V_{GS1} \]

\[ V_S \]

\[ \text{Norton equivalent} \]
\[
\begin{align*}
I_n &= \Delta qm_2 V_{ic} - \Delta qm_1 V_s - \frac{1}{R_{o1}} V_s \\
V_s &= 2R_{o3} \cdot I_n \\
\Delta qm_1 &= \frac{\Delta qm_1}{1 + (\Delta qm_1 + \frac{1}{Z_3}) 2R_{o3}} \\
&\text{where} \quad \Delta qm_1 \gg \frac{1}{R_{o1}} \\
&\text{Impedance at the output port} \\
&\text{with} \quad V_{ic} = 0 \\
A + \text{At freq.} \quad V_{ic} &= 0 \\
R_n &= R_d = 2 \cdot R_{o3} + R_{o1} \left(1 + \Delta qm_1 \cdot 2R_{o3}\right) = \Delta qm_1 \cdot R_{o1} \cdot 2R_{o3} \\
&\text{Common-mode equivalent half circuit (at At freq.):} \\
\text{Gm} &= \frac{\Delta qm_1}{1 + \Delta qm_1 Z_3} \\
\end{align*}
\]