Electronic measurements
Laboratory guide – Part A

Academic year 2025-2026

A. Pozzebon

Contents

Chapter 1

Measuring linear amplifier distortion

Instrumentation

- signal generator: Keysight 33600A, or Agilent 33220, or Tektronix AFG 3021
- digital oscilloscope: Keysight DSOX 1102G, or MSOX 3024T, or Agilent MSO 6012A
- audio frequency amplifier (second-order bandpas)
- power supply

1.1 Introduction

The output of a linear amplifier may suffer from distortion occurring due to non linearities within its circuits. Non-linear distortion depends on signal amplitude and, since it alters the *shape* of a signal, it also produces changes in its spectral composition.

Indicating by $V_{RMS(1)}$ the RMS value of a test sinewave at the fundamental frequency and by $V_{RMS(i)}$ the RMS value of the i-th harmonic, **total harmonic distortion** (THD) is calculated as follows:

$$THD[\%] = \frac{\sqrt{\sum_i V_{RMS(i)}^2}}{V_{RMS(1)}} \cdot 100 \tag{1.1}$$

or:

$$THD[\text{dB}] = 20\log_{10}\left(\sqrt{\sum_i V_{RMS(i)}^2}\right) - 20\log_{10}\left(V_{RMS(1)}\right). \tag{1.2}$$

Distortion measurements using sinewaves as test inputs can be carried out using the Fourier analysis mathematical function provided in most digital sampling oscilloscopes (DSOs). When a sinusoid is measured and the spectrum

trace is displayed on an oscilloscope screen, the frequency can be determined by positioning a horizontal cursor to coincide with the spectral peak and directly reading its position on the frequency axis.

Placing a vertical cursor over the peak in the displayed trace will yield a direct reading of RMS amplitude, usually given by a logarithmic scale in dBV:

$$\hat{X}_{RMS}[\text{dBV}] = 20 \log_{10} \frac{\hat{X}_{RMS}[\text{V}]}{1[\text{V}]}.$$

It has to be remembered that amplitude accuracy is affected by window shape through $W(\delta)$ and the normalized frequency distance δ. When $\delta = 0$ the amplitude estimate is correct, since $W(0) = 1$. For $0 < |\delta| \leq \frac{1}{2}$ one has $W(\delta) < 1$, therefore $\hat{X}_{RMS} < A_0/\sqrt{2}$. This attenuation, called *scalloping loss*, is a characteristic parameter that depends on the window shape.

Since the normalized distance δ is not known *a priori*, the largest possible deviation from the correct value should be considered. This is obtained when $\delta = \frac{1}{2}$, which gives the **worst-case scalloping loss** (WCSL).

When a signal is composed of several sinusoidal components, its DFT spectrum has multiple peaks. If the peaks are well separated along the frequency axis, each component can be measured independently.

Two aspects need to be considered, *peak detection* and *measurement*. The former relates to the ability to recognize the presence of distinct components even at minimum frequency separation. This feature is called **frequency resolution** and is *defined* as the minimum separation at which two *equal amplitude* sinusoidal components create *distinct* peaks in the spectrum trace.

If the displayed peak positions are close, interference may occur due to spectral leakage, that can affect both frequency and amplitude measurements. When sinusoidal components with different amplitudes are measured, spectral interference caused by leakage may affect measurement accuracy, since contributions from different signal components can combine, with partly unpredictable results. Furthermore, *masking* effects might cause smaller components to be hidden by the larger ones, thus remaining undetected.

To assess these effects, further information about the overall *shape* of the window are needed. These are usually given by:

- the normalized main lobe width;
- the attenuation of the largest side lobe with respect to the main lobe;
- side lobe fall-off with frequency.

The most significant parameters for some of the commonly employed window functions are summarized in Table 1.1.

Description

In this laboratory exercise the distortion of an audio-band amplifier will be measured at different values of the input sinewave amplitude. A final optional step deals with measurement of intermodulation distortion (if present).

The oscilloscope Fourier analysis function set-up allow a choice of both the *frequency span* (F_{span}) and the *centre frequency* (F_{centre}). This means the

Table 1.1: Parameters characterizing windows in common use for DFT-based spectral analysis.

Window	WCSL [dB]	minimum side lobe attenuation [dB]	main lobe width [bin]	$2{\cdot}B_{-6dB}$ [bin]	ENBW [bin]
uniform	3.92	13	2	1.21	1
Hann (*Hanning*)	1.42	32	4	2	1.5
Blackman-Harris	1.13	71	6	2.27	1.71
flat-top	< 0.01	93	10	4.58	3.77

minimum frequency is not constrained to be zero so that, besides $0 \leq f \leq F_{span}$, any other interval $F_{centre} - \frac{F_{span}}{2} \leq f \leq F_{centre} + \frac{F_{span}}{2}$ can be analyzed.

Vertical axis

A logarithmic scale (**dBV**) is employed for the vertical axis. Absolute RMS voltage values are converted into a log-ratio value by taking 1 V RMS voltage as the reference value. This means an absolute value V_x on the amplitude spectrum is given in dBv as:

$$V_x[\text{dBV}] = 20 \cdot \log_{10} \frac{V_x[V_{RMS}]}{1[V_{RMS}]} \tag{1.3}$$

while the vertical scale factor is given in dB/div.

The **reference level** is the absolute amplitude value (in dBV) associated to the vertical axis middle point on the screen. Consequently, by varying the reference level the spectral trace is vertically shifted up or down on the display. Vertical cursors automatically take such variations into account, so that a direct reading (dBV value) is always provided.

Two preliminary assessments are needed before measuring the device under test, namely:

- the verification of DSO performances, as related to spectral analysis.
- an approximate estimate of bandwidth for the amplifier under test;

1.2 Oscilloscope distortion

It has to be emphasized that, although digital oscilloscopes may be able to provide spectral measurements, their hardware design is optimized for *time-domain* measurement. Therefore, input channel and data acquisition performances like sensitivity, noise and linearity *do not match those of a dedicated spectrum analyzer*. A spectrum analysis tool does provide useful insight on measured data, but users also need to be aware of its limitations.

Distortion measurements are aimed at detecting signal components at different frequencies from the input signal. For this reason it is necessary to first

check for distortion within the measuring instrument itself, to ensure any spurious response is not mistakenly attributed to the device under test.

Some degree of distortion may actually occur within the oscilloscope, for instance due to non-uniformity of the ADC quantization characteristic, or because of moderate non-linearity in the input channel. These effects also produce harmonics, appearing as peaks in the spectrum trace. To avoid ambiguity, instrument distortion needs to be checked *first*, using a low-distortion sinewave as the test input.

For this test, the generator output should be connected directly to the DSO input. Test **frequency and amplitude** are suggested to be in the **same** range that will be used for amplifier testing. Both noise and distortion should be negligible in the test generator, that is characterized in this regard by the **signal to noise and distortion** (SINAD) parameter, defined as the ratio of the RMS value of the sinusoidal component at fundamental frequency, to the RMS value of noise plus distortion. A typical generator with digitally synthesized output ensures SINAD in the order of 70 dB, which is then the lower limit for oscilloscope characterization.

WARNING For low-level signals, worse values of SINAD might be found. Always check signal generator set-up before this test.

1. Set the same DSO vertical scale factor that will be employed to measure the amplifier output and select the desired test frequency f_{Test}. Adjust the sinewave amplitude so that the displayed trace extends over the whole instrument input range (that is, the trace should almost fill the screen), so that the full input range of the ADC will be tested.

   WARNING: the sinewave peak-to-peak amplitude should be *close* to the oscilloscope input range *without* exceeding it. Otherwise, the ADC will be overloaded, numerical output values will saturate and the computed spectrum will be distorted.

2. The required indication, that characterizes the instrument for the purposes of this test, is the difference (in dB) between the magnitude of the spectral peak at the test frequency and that of the largest harmonic produced by the instrument. This defines the *spurious-free dynamic range*, that is, the range of amplitude values within which a spectral line may be attributed with certainty to distortion by the device under test.

3. Suggested indicative instrument settings for this test:

   - *center frequency*: $\cong 5 \cdot f_{Test}$;
   - *frequency span*: $\cong 10 \cdot f_{Test}$;
   - vertical scale factor: 10 dB/div.

   The DSO horizontal scale factor should be adjusted so that the measured spectrum can cover the entire frequency range of interest. It should be remembered that the frequency step is inversely proportional to the oscilloscope observation interval and, in general, this should allow the acquisition of a sufficiently high number of sinewave periods.

Ideally, the spectrum of a sinusoidal wave is displayed as a single spectral line (image components are not displayed by the instrument), therefore discrepancies from the ideal behavior are easily evidenced. The spectral tarce displayed by the instrument will include a large peak at the test frequency, a broad band white noise component and, possibly, a few spectral lines caused by distortion within the instrument.

Noise floor

Broad band noise in the observed trace is the result of two separate and independent contributions:

- signal **quantization**;
- electrical **noise** introduced by the input channel stages.

Their combination can be described by a random process whose variance σ^2_{DSO} is the sum of the variances of the two independent components. Its power spectral density is constant and independent of frequency. It can be estimated as the mean value of the set of points on the spectrum trace where only noise is present and is called the **noise floor** (NF).

Noise floor level is generally comparable with possible spectral components introduced by oscilloscope distortion. These can be better evidenced by the use of the *high resolution* acquisition mode, that significantly reduces the displayed noise floor.

1.3 Device under test bandwidth evaluation

This measurement should provide an approximate estimate of the frequency band of interest. Steps are briefly described as follows:

1. once the amplifier is powered up, a sinusoidal waveform should be selected from the signal generator. Using a 'T' coaxial connector and two coaxial cables, the signal is sent in parallel to the amplifier and to one of the oscilloscope inputs that provides a visual check;
2. the amplifier output is also to be connected to one of the oscilloscope input channels;
3. input signal amplitude should be adjusted to avoid any visible sign of distortion at the amplifier output;
4. reference points for the amplifier frequency response can be determined as follows:
    - at the **centre frequency** amplifier gain is maximum (maximum amplitude of the output signal, assuming the input remains constant) and the output sinewave is in opposition to the input (i.e., a 180 degree phase shift);
    - at the **-3 dB cut-off frequencies**, both lower and upper, the output sinewave amplitude is approximately 30% smaller than at the centre frequency.

To help find these, it may be useful to compute the value corresponding to 70% of the peak-to-peak amplitude at centre frequency. Then, using vertical cursors, a visual reference can be created on the display, so that the -3 dB condition is readily evidenced as the generator frequency is varied.

Approximate values of the three frequencies suffice to set-up distortion measurement.

1.4 Measurement of harmonic distortion

Total harmonic distortion (THD) is defined as the ratio of the cumulative RMS value of harmonic components to the RMS value of the sinusoid at fundamental frequency. Determination of THD requires the analysis of the amplifier output to measure the RMS avlues of the fundamental and harmonic components. THD value may be expressed in percent, or in dB.

The RMS value of a sinusoidal component is obtained by direct reading, after positioning a vertical cursor on the corresponding spectral peak top. The value in dBV may be converted into RMS voltage by the inverse relationship:

$$V_{RMS}[\text{dBv}] = 10^{\frac{V_{RMS}[\text{dBV}]}{20}} \tag{1.4}$$

Any spectral line at harmonic frequencies can likewise be directly measured by a cursor reading and converted back in RMS value using (1.4).

Using a spectral window with a low value of *scalloping loss* ensures better agreement between the measured spectral peak and the actual RMS value of the sinusoid.

Indicating by $V_{RMS(i)}$ the RMS value in V of the i-th harmonic and by $V_{RMS(1)}$ the RMS value at the fundamental frequency, THD is calculated by (1.1), or (1.2).

WARNING: remember that quantities expressed in a logarithmic scale **have to be converted back into linear** before using values for the distortion term (numerator in the ratio) in the equations referenced above.

Measurement steps

- Select a sinusoidal waveform shape on the signal generator. **Frequency** should be set to a value within the amplifier bandwidth, **close to the high-frequency cut-off**.
- Connect the generator output to the amplifier input and (using a 'T' coaxial connector) to one of the oscilloscope input channels. Connect the amplifier output to another oscilloscope input channel. collegare l'uscita del generatore di funzione all'ingresso dell'amplificatore in banda audio. Waveform **amplitude** should be checked to avoid distortion at the amplifier output – a visual check may suffice. A good starting point for the measurement is *just before* clipping caused by output saturation becomes visible, remembering that 1% THD remains unnoticed by visual inspection.

- Activate the oscilloscope spectral analysis function, **employing the high-resolution acquisition mode**. Set up *frequency span* and *centre frequency* so that each sinusoidal component of the signal can be singled out. I

Measurement should be repeated for a few different input signal amplitudes and frequencies, so that an idea of the dependence of output THD from amplitude and frequency can be obtained.

Note: after each variation, it is important to check that the output signal is still displayed correctly and, if necessary, the vertical scale factor must be varied to ensure no signal distortion is caused by clipping in the instrument own input channel.

At each iteration, the following operations need to be carried out:

1. using cursors, measure the amplitude and frequency of the largest visible spectral component. Check that its freqeuncy corresponds to the generator setting;

2. using cursors, measure the amplitude and frequency of the most significant harmonic components (if any). **Remember** that any spectral component that is found to be smaller than the largest harmonic by 10 db or more, becomes *irrelevant* in (1.1) and (1.2) – you do not need to measure it;

3. compute THD using (1.1) or (1.2).

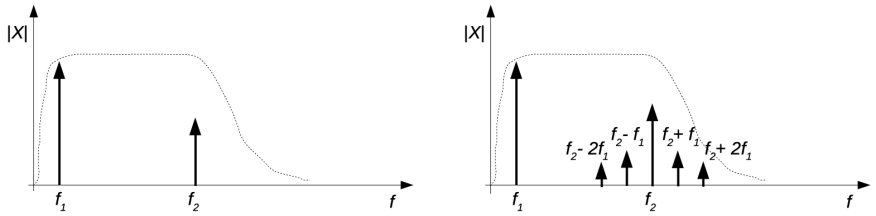
1.5 Analysis of intermodulation distortion (optional)

(**Note**: for this measurement a Keysight 33600 generator is required. Alternatively, a Hewlett-Packard 8904A generator should replace Agilent 33220 or Tektronix AFG 3021).

Intermodulation methods are based on the simultaneous use of **two** sinewaves at different frequencies as the test input. **If intermodulation distortion occurs** because of non-linearity in the device under test, the output signal will include measurable intermodulation components. One of the possible methods is presented in the following.

WARNING: since the test signal is a *sum* of sinewaves, its peak-to-peak amplitude may exceed that of the individual components and, as a worst case, will be equal to the **sum of the two component amplitudes**. It is essential to check **first** that no clipping occurs, neither at the amplifier output, nor on the oscilloscope display. Otherwise the oscilloscope vertical scale factor needs to be adjusted and, if necessary, test signal amplitude should be suitably reduced.

The test signal is the sum of a low-frequency and a high-frequency sinewave. The lower frequency $f_1$should be slightly greater than the low-frequency cut-off in the amplifier response. The higher frequency f_2 should be closer to the high-frequency cut-off. Expected non-linearity effects are illustrated in Fig. 1.1. Intermodulation components, ***if present***, can be found at frequencies: $f_2 \pm k f_1$, with k an integer.



(a) input spectrum (b) output spectrum

Figure 1.1: Analysis of intermodulation distortion: first method.

Interharmonic distortion, like THD, may be expressed either in percent or in dB and in this case is the ratio of the RMS value of distortion components to the RMS value of the high-frequency sinewave:

$$D_1 = \sqrt{\frac{V_{f_2-2f_1}^2 + V_{f_2-f_1}^2 + V_{f_2+f_1}^2 + V_{f_2+2f_1}^2 + ...}{V_2^2}}$$

Settings for the Keysight 33600 signal generator:

- using the **Waveform** functional key, select a sinusoidal shape and input the settings for the low-frequency (f_1) component;
- from the **Modulation** menu, select the item **Type**, the modulation mode **Sum**;
- set configuration parameters for the modulation waveform to a sinusoidal **Shape** and select the frequency (f_2) and amplitude, using respectively menu items **Sum Freq** and (**Sum Ampl**). The latter is provided as *percent* of the first sinewave, for instance, a 100% value should be input to obtain equal-amplitude components;
- activate modulation (**Modulate** − **On**)

A suggested spectral analysis setting that enables to measure these components might be a *centre frequency* equal to f_2 with *frequency span* $10 \cdot f_1$. Of course, only components within the instrument *spurious-free dynamic range* can be safely considered intermodulation products.

Chapter 2

Time-domain reflectometry (TDR)

Instruments

- Keysight 33600A or Tektronix AFG 3101 signal generator;
- coaxial cable;
- Keysight DSOX1102G (100 MHz) or MSOX3024T (200 MHz) digital oscilloscope;
- accessories and passive components.

2.1 TDR – Laboratory activity

This laboratory exercise presents a few typical test conditions, that are analyzed and interpreted to provide introductory experience on the use of time-domain reflectometry as a diagnostic tool. "Transmission lines" are represented by ordinary coaxial cables with lengths of some tens of meters, which allows to carry out the exercise with standard laboratory instrumentation. In practice, interconnects in an electronic board often take the form of *microstrip lines* whose lengths are in the order of some tens of millimetre. Time resolution in measurement thus needs to be scaled accordingly and, as a consequence, broader band instrumentation is required. TDR principles remain the same and can be usefully illustrated by this exercise.

A TDR measuring system is composed of:

- a broad-band signal generator, providing either short pulses or steps with short rise time, whose output impedance should match the characteristic impedance of the transmission line under test.

  Since coaxial cables with characteristic impedance $Z_0 = 50\Omega$ are employed in the exercise, a standard laboratory generator with 50Ω output impedance can be employed;

- an oscilloscope with comparable bandwidth, that is connected to the line under test in parallel to the test signal generator.

Measurement set-up

A **square wave** should be selected as the generator output. Amplitude can be chosen at will (suggested, **around 1 V**), whereas waveform period should be long enough to avoid superposition of the TDR responses from consecutive voltage steps. Any fundamental frequency not greater than **about 10 kHz** should be good for the purpose and this can be checked by observing TDR waveforms on the oscilloscope.

To avoid any disruption of generator to line impedance matching, the oscilloscope must be employed in the **high impedance** (1 MΩ) input configuration. For the same reason, connection between the oscilloscope and the line under test should be kept as short as possible. A simple solution is placing a 'T' connector directly on the oscilloscope input, with the coaxial cable line feeding through it.

2.1.1 Measuring the length of a line

A coil of coaxial cable is provided for this exercise. For measuring length, it suffices to connect one end of the cable to the 'T' connector, keeping the opposite end open. This produces total reflection of the test step waveform (with an open cable $Z_L = \infty$ and the reflection coefficient is $\rho = 1$), that propagates back to the oscilloscope and the generator. The reflected wave has the same height as the incident wave, therefore the steady-state voltage measured by the oscilloscope in the generator no-load output voltage.

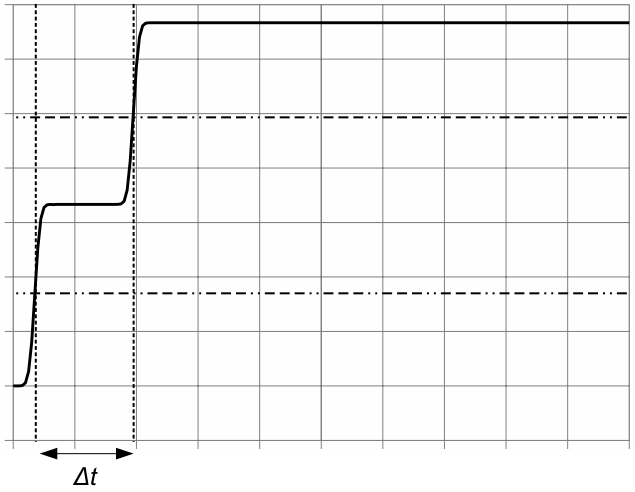


Figure 2.1: TDR measurement of an open line ($R_L = \infty$).

The length of the line is calculated after measuring the delay between the incident wavefront and the reflected wavefront, as shown in Fig. 2.1. Using cursors, the reference position should be the middle point of each rising edge.

The measured interval Δt is the time needed for the round-trip travel along the line (from one end to the other, and back) at the propagation speed $v = c/\sqrt{\epsilon_r}$, where $c \cong 3 \times 10^8$ m/s is the speed of light in vacuum and ϵ_r is the dielectric constant of the medium where the electromagnetic wave is propagating. In this case the dielectric constant of the coaxial cable insulation material

should be considered, with $\epsilon_r = 2.3$ for polyethylene the corresponding speed is about 20 cm/ns (more precisely, 19.8 cm/ns).

Verification of length measurement accuracy

TDR measurements can provide rather accurate length measurements. In fact, the use of a steep voltage edge enables to accurately locate waveform features on the displayed time-domain trace. This is now verified by an *incremental* measurement, where a cable of known length is joined to the longer cable and the length difference is measured by TDR. The added cable segment is short enough to allow it to be measured by an ordinary measuring tape, so that the two length values can be compared.

For this measurement a coaxial cable, approximately 1-2 m in length, is connected to the end of the cable coil by a BNC(F) to BNC(F) adapter and a new end-to-end length measurement is taken. This yields a new, larger time interval value $\Delta t'$, since total length is greater. The "electrical" length of the added cable can be determined from the difference $\tau = \Delta t' - \Delta t$.

The resulting length value should agree, within few millimeters, with the value obtained by using the measuring tape.

The factor limiting accuracy in this measurement is the time resolution Δ_t of the horizontal cursors on the oscilloscope display. **Determine the resulting uncertainty on the measurement of cable length.**

Note: the length of the added cable is determined by measuring a time *difference* τ. In principle, it should be possible to measure it directly, but the short length of the cable (made necessary by the need for comparison with a measuring tape) makes this measurement more difficult. Since for a short cable propagation round-trip time is not much longer than the test signal rise time T_r, the two steps shown in Fig. 2.1 would be much harder to discern accurately in this case.

2.1.2 Line termination impedance

Connect the BNC to crocodile clip adapter to the free end of the cable coil. Clips can be used to connect different types of passive components such as resistors and capacitors, as line termination loads.

Note: the effect of the adapter connector impedance may also be visible.

Resistive load

With a matched load connected at the end of the cable (that is, $R_L = |Z_0|$) the reflection coefficient ρ is zero an no reflection occurs. Otherwise, the amplitude of the reflected wave can be easily obtained after calculation of the reflection coefficient. For a resistive load, the final steady state value on a TDR trace is:

$$E_i(1+\rho) = E_i\left(1 + \frac{R_L - Z_0}{R_L + Z_0}\right)$$

If resistors from the standard E12 series are employed, the nominal value closest to the impedance matching condition is $R_L = 47\Omega$. In this case $\rho =$

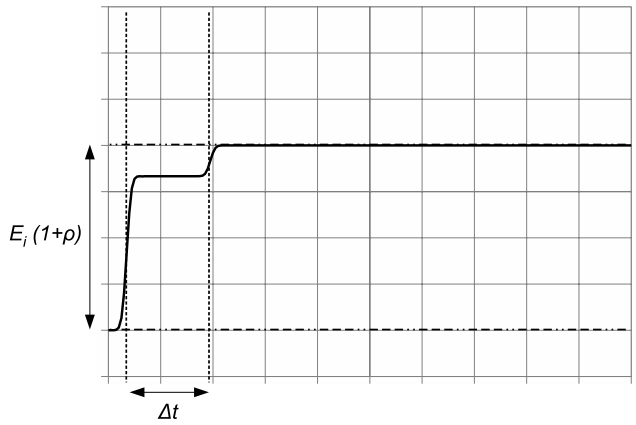


Figure 2.2: TDR measurement for a line with resistive load $R_L \neq |Z_0|$).

-0.031 therefore, after time Δt, only a small reduction of waveform amplitude will occur.

The TDR measurement should be repeated **with other values of** R_L.

Capacitive load

When the load impedance includes a reactive component, the TDR waveform will evidence transients related to reactance in the load. In this part of the exercise, the cable is terminated by a capacitor to show the effect of reactance.

Using the adapter clips, connect a capacitor C_L at the end of the cable. After time Δt, the TDR waveform follows an exponential trend, that is typical of capacitor charging in a RC circuit. In this case, load capacitance C_L is charged through the generator output resistance, that is equal to Z_0:

$$v(t) = 2E_i \left(1 - e^{-\frac{t}{Z_0 C_L}}\right)$$

An estimate of the load capacitance can be obtained if the exponential time constant $Z_0 C_L$ is known. A sufficiently accurate approach is based on measuring **time to half-value** $t_{\frac{1}{2}}$, that is, the time it takes for voltage across the (initially uncharged) capacitor to reach half of its final value (Fig. fig:TDR-C). The following relationship:

$$e^{-\frac{t}{Z_0 C_L}} = \frac{1}{2} \qquad \text{from which:} \qquad Z_0 C_L = \frac{t_{\frac{1}{2}}}{\ln 2} \cong t_{\frac{1}{2}} \cdot 1.44$$

then allows to determine C_L.

The resulting value should be compared with the capacitor nominal value, accounting for manufacturing tolerance that may be up to 10% in a common commercial grade component.

Visualizing source mismatch and multiple connections

Getting a "visual feeling" for various TDR plots can be a useful aid in interpretation. Some tests are suggested here.

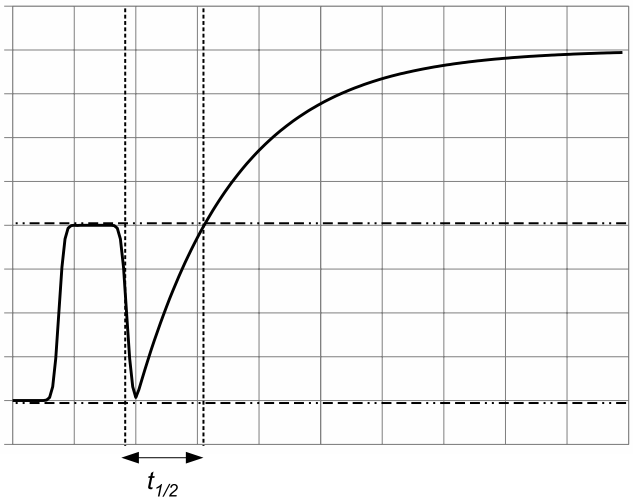


Figure 2.3: TDR measurement for a line with capacitive load: determination of time to half-value $t_{\frac{1}{2}}$.

1. To understand the effect on TDR measurement of source mismatch, a resistor R_d can be intentionally added in series to the generator output, so that the equivalent output resistance will rise to $R_g + R_d$. For instance, taking standard value $R_d = 150\Omega$ the equivalent resistance is 200 Ω and a mismatch with the coaxial cable characteristic impedance Z_0 is created.

   If the cable coil is now connected again to the 'T' connector, leaving the opposite end open, it will become apparent that reflected power is not instantly absorbed back into the generator. Further reflections, with progressively increasing amplitude, take place until the final value $2E_i$ is eventually reached. In this case, however, a much longer transient is caused by the succession of reflections that take place on the generator side.

2. The effect of multiple connections can be displayed by using a second 'T' coaxial connector, with a BNC(F)-to-BNC(F) adapter, to enable the connection of **two** short cables in parallel at the end of the line. If their ends are now left open, total reflection will occur on both, but for a short time the TDR trace will first evidence a drop in amplitude, consequent to the fact that two 50-Ω cables in parallel are equivalent to a resistance of 25 Ω.

   Further variants can be now created by using different termination loads on either cable (for instance, a 47-Ω resistor could approximate a matched load on one of them).

Chapter 3

Characterization of a *Phase Locked Loop*

Strumentazione

- Keysight 33600A signal generator;
- Keysight MSOX 3024T digital oscilloscope;
- PLL test board.

3.1 Introduction

The analysis of a complex device for characterization or diagnostic purposes presents a number of diverse issues, where both designer and test engineer skills are involved:

- understand device operating principles to establish the expected behavior, based on which deviations leading to possible malfunctions can be evidenced;
- define suitable test points and execute measurements to determine the actual device behavior;
- determine the dependability of test indications by analyzing features and performances of measuring instrumentation.

It is hardly possible to deal with multidisciplinary problems of this kind in terms of general principles. This exercise provides one example among many possible circuit applications. A phase-locked loop (PLL) has been chosen as the object of the test on account of its relevance to measuring instrumentation and because this kind of circuit is widely employed in general.

3.2 *Phase Locked Loop* – operating principle

A *phase locked loop* (PLL) is a feedback system with the ability to track a periodic input and produce an output signal having the *same* fundamental frequency or, more generally, a fundamental frequency whose ratio to the input

frequency is a rational number. PLLs are widely employed as frequency multipliers, FM and FSK demodulators, clock recovery circuits in communications systems, etc..

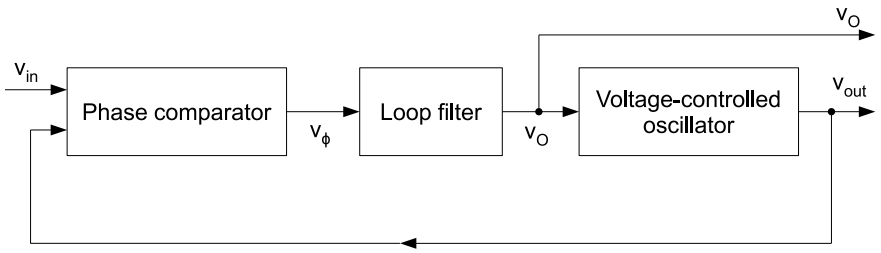


Figure 3.1: Generic PLL block diagram.

The block diagram of a generic PLL system, shown Fig. 3.1, is composed of three elements:

- a *phase comparator*, that compares the **instantaneous** phase of the input signal $v_{in}(t)$ with the instantaneous phase of the signal $v_{out}(t)$ generated within the PLL by a voltage-controlled oscillator. The phase comparator output is a voltage signal $v_\phi(t)$, whose mean value is proportional to the phase difference between the two inputs;
- a *loop filter* having a low-pass frequency response, whose output is the mean value of $v_\phi(t)$;
- a *voltage controlled oscillator* (VCO), that produces a periodic signal whose fundamental frequency is *proportional* to the value of the input voltage. The loop filter output voltage $v_O(t)$ is employed as the VCO control voltage.

A simplified description allows a basic understanding of the system. Considering sinewaves for simplicity, assume that the frequency f_{in} at the PLL input differs from the frequency f_{out} of the signal produced by the VCO. Then, even with a slight frequency difference, the difference in phase between the two signals will vary with time. The VCO input voltage $v_O(t)$ is in turn proportional to the difference of frequency and instantaneous phase between $v_{in}(t)$ and $v_{out}(t)$.

Let the input signal $v_{in} = A\sin(2\pi f_{in}t + \phi_{in})$ and the VCO output $v_{out}(t) = A\sin(2\pi f_{out}t + \phi_{out})$ be at different frequencies. The instantaneous phase difference:

$$\Delta\phi(t) = [2\pi(f_{out} - f_{in})t + \phi_{out} - \phi_{in}]_{mod(2\pi)} \,. \tag{3.1}$$

is a periodic quantity, whose period is 2π radians. Within one period, $\Delta\phi(t)$ is either increasing or decreasing linearly with time, depending on whether it is $f_{out} > f_{in}$ or $f_{out} < f_{in}$.

A phase comparator may then be described by the relationship:

$$v_\phi(t) = K_\phi \cdot \Delta\phi(t) \qquad \text{with:} \qquad |\Delta\phi(t)| < \pi \tag{3.2}$$

where the constant K_ϕ is given in [V/rad]. This means that the phase comparator output can be considered a *sawtooth* waveform with period $T_\phi = [1/(f_{out} -$

f_{in})]. As long as the difference between the two frequencies remains constant, that is, assuming no feedback in the PLL circuit, the phase comparator output voltage would keep varying linearly within its range with period T_ϕ, as illustrated by Fig. 3.2.

This condition occurs when no signal is present at the PLL input, in which case the VCO settles to a steady output frequency, called the *free-running frequency* (FRF). The FRF value is determined by the characteristics of all PLL building blocks, particularly by the behavior of the loop filter. When lock to the input frequency is lost, the PLL also settles into a similar condition.

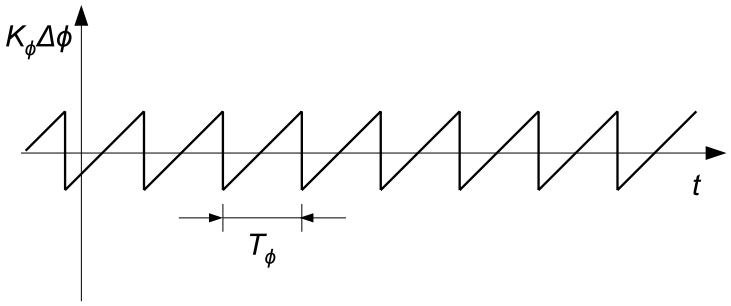


Figure 3.2: Phase comparator ideal output voltage when the two periodic inputs have different fundamental frequencies (ramp slope can be either positive or negative, depending on which frequency is higher).

As VCO control voltage varies, feedback in the system of Fig. 3.1 should tend to reduce the difference between the output and the input frequencies. Indeed, when f_{out} is close enough to f_{in} the VCO gets "locked" onto it. An indication of the phase comparator output voltage behaviour is provided by the plot in Fig. 3.3, where input frequency is assumed to remain constant. The final steady state voltage corresponds to the control input at which the VCO produces the desired frequency, therefore the input-output phase shift in the lock condition depends on frequency. A behaviour of this kind is exemplified by the *Phase Comparator I* circuit within the integrated circuit employed for this laboratory exercise.

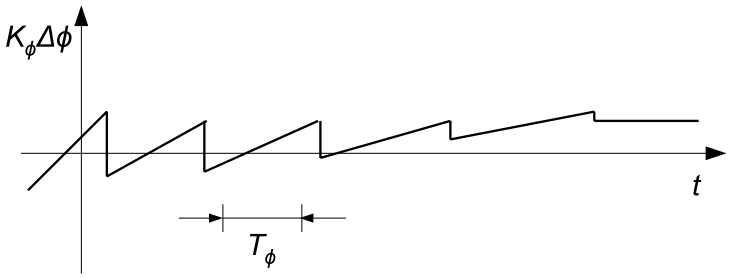


Figure 3.3: Phase comparator ideal output voltage when the PLL is locking onto the input signal.

If the VCO input voltage range and the phase comparator output range coincide, the PLL might be able to lock to the input signal over the whole VCO frequency interval. The actual interval may be narrower and depends on

loop filter characteristics, so that **two** different interval definitions need to be considered:

- **Lock range** – if the input frequency varies, a PLL can **track** its variations as long as they remain within a certain interval called the **lock range**. This kind of behavior makes a PLL circuit also useful as a frequency demodulator. In a frequency-modulated (FM) signal information is encoded into frequency variations, that a PLL can translate into a proportional variable voltage at the loop filter output.

- **Capture range** – this refers instead to the PLL ability to lock onto the input frequency and track it, starting from a VCO free-running state, that is, an out-of-lock condition. It can be realized that the condition is more demanding compared to the lock range definition. Capture range is determined by phase comparator and loop filter characteristics, it may be as wide as the lock range, but in practice capture is harder than keeping lock and the range is often narrower.

3.3 Measured device

The device employed for this exercise makes use of a CD4046B integrated circuit (IC). This is a CMOS technology component design for the implementation of phase-locked loop circuits. Its layout and pin disposition are shown in Fig. 3.4. The device provides a voltage-controlled oscillator with square wave output and a choice of two different phase comparators.

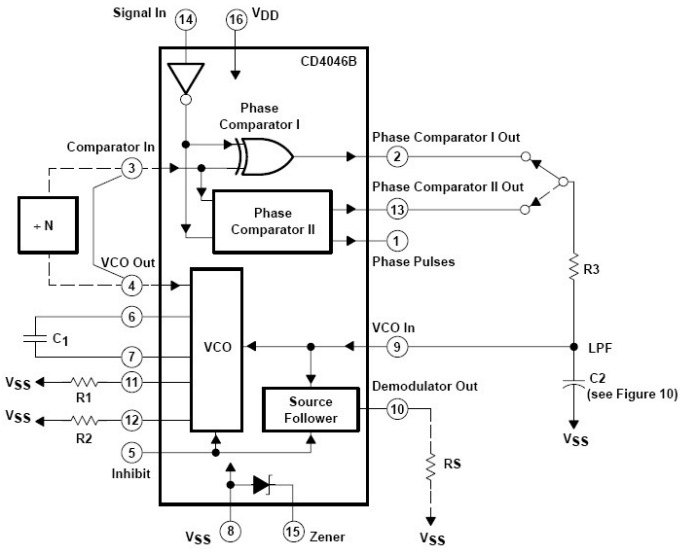


Figure 3.4: Block diagram of CD4046B integrated circuit. *From: Application Report SCHA002A - February 2003, Texas Instruments.*

3.3.1 *Voltage controlled oscillator*

The VCO in the CD4046B IC is a square wave oscillator realized by feedback-connected logic inverters. To set the output frequency range, an external resistor and an external capacitor, shown as R_1 and C_1 in Fig. 3.4, need to be added. Another resistance, R_2, may optionally be employed to set a non-zero minimum frequency value.

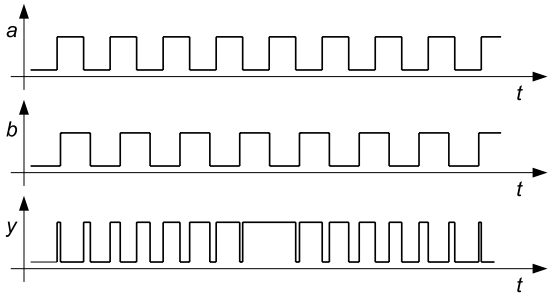
Circuit power supply voltage is V_{DD}, whereas $V_{SS} = 0$. VCO control voltage can vary between 0 and V_{DD}, although the useful range where a proportional output frequency is obtained is smaller and needs to be determined by measurement.

To obtain a complete PLL it suffices to realize an external loop filter through which the VCO output is fed back into the phase comparator. A simple design can be realized by passive components, like the capacitor C_2 and resistance R_3 shown in Fig. 3.4.

3.3.2 *Phase comparator I*

Phase comparator I is a simple exclusive-OR (XOR) logic gate. Its inputs are the PLL input signal and the VCO output. Recalling the logic behavior of an XOR gate, it can be realized that it produces a kind of "product" between the two signals, similar to the operation of a multiplier or a balanced mixer. It is useful to consider two conditions that help better understand operation of the XOR as a phase comparator:

- if the two inputs are at the same frequency, the XOR gate output is a square wave at the same frequency, having *a duty cycle proprotional to the phase shift* between them;
- if the two inputs are at different frequencies, f_{in} and f_{VCO}, the XOR gate output is a square wave whose duty-cycle varies at frequency $|f_{in} - f_{VCO}|$. The behaviour is illustrated by Fig. 3.5.



a	b	y
0	0	0
0	1	1
1	0	1
1	1	0

Figure 3.5: time diagram showing input and output signals for an XOR-based phase comparator and truth table of a two-input XOR logic gate.

The output of *Phase comparator I* is averaged by the loop filter to extract a continuous or slowly varying component, that is needed to control the VCO. As shown by the plot in the lower part of Fig. 3.6, where a simple RC filter is shown, phase shift is linearly related to voltage in the interval $(-\pi, \pi)$.

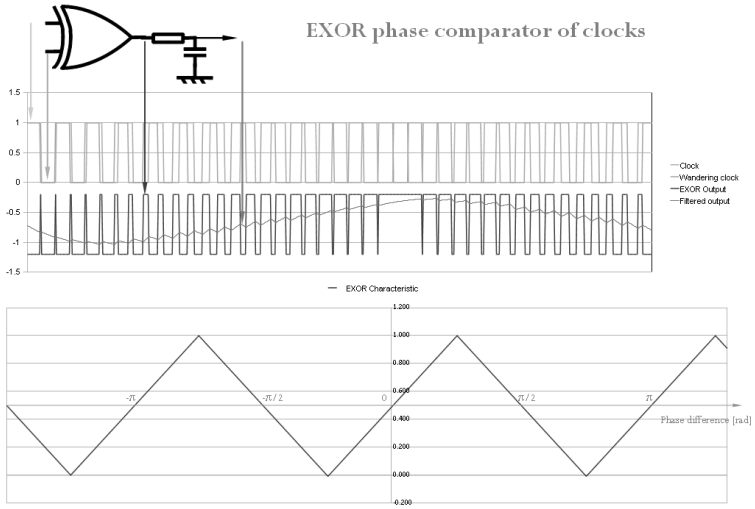


Figure 3.6: Operating principle of an XOR-based phase comparator. From *Wikimedia Commons.*

If no signal is present at the PLL input, or when the circuit is out of lock, the mean voltage at the output of *Phase comparator I* is $V_{DD}/2$. The VCO output will correspond to this voltage input, that determines the PLL *free-running frequency*. When the PLL has locked to the input, the phase shift of the VCO output is constant and depends on the generated signal frequency.

Phase comparator I has the advantage of simplicity, but also suffers from some limitations, namely:

- the loop filter output tends to be affected by ripple, that can affect the output frequency stability. This requires care in the loop filter design, whose bandwidth should be narrow enough to limit *jitter* to an acceptable level;
- the XOR gate output varies its duty cycle at a frequency that depends on the difference $|f_{in} - f_{VCO}|$ between the two phase comparator inputs. If the PLL is out of lock and the difference $|f_{in} - f_{VCO}|$ is beyond the loop filter bandwidth, the PLL will not be able to lock on the input.

Consequently, in a PLL where *Phase comparator I* is employed "capture" is possible as long as the input freqeuncy is not too far from FRF. Once lock has been achieved, however, the input freqeuncy can vary over a much wider range, possibly up to the whole VCO output range. In other words, in this case capture range is narrower than lock range.

IMPORTANT
For correct operation, the input to the XOR-based Phase comparator I should be a **waveform with 50% *duty cyle***, that is, the positive and negative part of its alternating component must have equal duration.

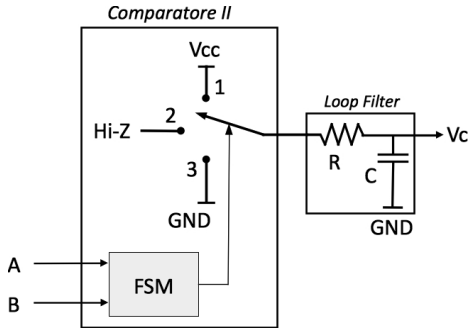


Figure 3.7: Phase comparator and loop filter based on edge detection.

3.3.3 *Phase comparator II*

The second phase comparator (*Phase comparator II*) is a sequential digital logic network that realizes a finite state machine (FSM). State changes are triggered exclusively by rising edge detection on the input signals and determine the transitions of a three-state output. The output is connected to an RC electrical network as the PLL loop filter (Fig. 3.7). The operation of Phase comparator II can be described in simplified form by assuming that the FSM controls the position of a three-way switch, enabling one of three possible outputs:

- power supply voltage V_{DD} (1 – logic output 'high' logic state): in this case, capacitance C is charged through resistance R;
- floating high impedance output (2 – logic output in 'high-Z' state): capacitance charge remains unchanged;
- ground (3 – logic output 'low' logic state), in this case, capacitance C is discharged through resistance R.

State transitions in the FSM take place according to the following rules:

- if a rising edge is detected on input 'A' (to which the reference input signal is connected), the state of the switch must be increased by 1;
- if a rising edge is detected on input 'B' (to which the feedback signal from the VCO is connected), the state of the switch must be decreased by 1.

It can be realized intuitively that the two operations correspond, respectively, to increasing or decreasing the VCO output frequency.

When the PLL is in a constant-frequency lock condition, the phase comparator output should ideally remain in the high-impedance state most of the time. Charge in the loop filter capacitance then changes little, since the VCO input impedance is also high. The filter "memory" thus retains the present VCO control input V_C, so that output frequencies remain equal and mutual phase shift is theoretically nil.

In practice, the edges of the two phase comparator inputs happen to be *nearly* simultaneous, which results in a continuous sequence of near-instant corrections. This avoids capacitance self-discharge (which would actually occur through the high-impedance connection) and ensures that the mean voltage on the capacitor

is indeed V_C. On the other hand, this causes slight perturbations that translate into small variations of the VCO output frequency.

Using Phase comparator II the capture range and lock range about coincide, regardless of the loop filter features. When the input signal is a square wave at frequency lower than f_{min} or higher than f_{MAX} the system output is at the respective limiting frequencies, whereas with no input the FRF is at lower end of the PLL operating range.

3.4 Circuit board for the laboratory exercise

The CD4046B IC and the required external components are mounted on a board (Fig. 3.8) with a 9-V power supply (V_{DD}). BNC connectors are provided at different test points on the circuit to enable the observation of waveforms.

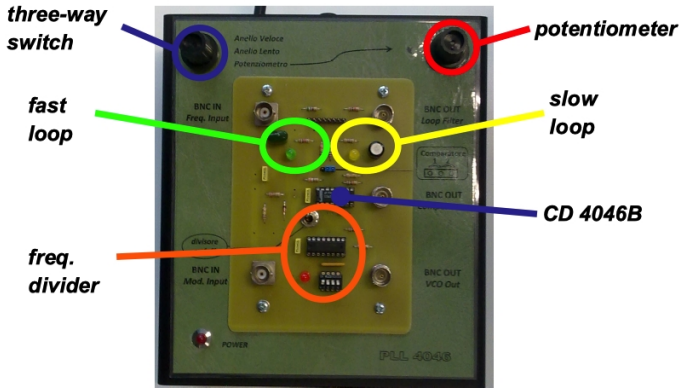


Figure 3.8: Circuit board for the laboratory exercise.

PLL circuit configurations can be modified by means of:

- a **three-position selector** that allows to choose the source of the VCO control voltage. In each position a corresponding colored LED is lit near the active components:
  - *Potentiometer* (**red LED**): the VCO is controlled through a linear potentiometer that allows to vary input voltage between 0 V and the power supply voltage ($V_{DD} = 9$ V). No feedback is provided and the VCO operates as an open-loop device;
  - *Slow loop* (**yellow LED**): the feedback loop is closed and the loop filter cut-off frequency is about 1 Hz;
  - *Fast loop* (**green LED**): the feedback loop is closed and the loop filter cut-off frequency is about 300 Hz.
- **Jumper**: the jumper placed in the centre of the circuit board allows the selection of either of the two phase comparators:
  - *left position*: *Phase comparator I*;
  - *right position*: *Phase comparator II*.

The circuit board also includes a *frequency divider* that can be included in the PLL feedback path by using a **toggle switch**. When the divider is active an **orange LED** is lit.

NOTICE The frequency divider can **only** be used when *Phase comparator II* is employed.

The waveform at the frequency divider output is not compatible with *Phase comparator I*, since the XOR gate requires that the duty cycle of input signals is about 50% to operate correctly.

The divider is programmed through a group of four microswitches that sets the binary value of the dividing factor M. Each switch is associated with a power of 2 (hence, 0, 2, 4 and 8) allowing to program in binary digits a number between 0 and 15. The actual dividing factor is obtained by adding 1 to this number, hence M varies from 1 (no division) to 16. By doing this, the phase comparator is presented with a feedback input whose frequency is f_{VCO}/M.

Since lock is obtained between the feedback signal and the input, the PLL in this case acts as a *frequency multiplier*, yielding: $f_{VCO} = f_{in} \cdot M$. When using frequency multiplication it has to be remembered that the VCO has a finite output frequency range (f_{min}, f_{MAX}), therefore the input frequency f_{in} should not exceed the range (f_{min}/M, f_{MAX}/M).

3.5 Exercise steps

A number of measurements have to be carried out *in sequence*, namely:

1. measure the VCO voltage to frequency characteristic;
2. determine the PLL capture and lock ranges;
3. observe the PLL step response and determine lock time;
4. (optional) using an FM modulated input signal, compare FM modulating waveforms (as set on the waveform generator) with the corresponding *loop filter* outputs.

The exercise board provides access to a number of test points through BNC connectors. Their position in the system block diagram and identifying names are shown in Fig. 3.9.

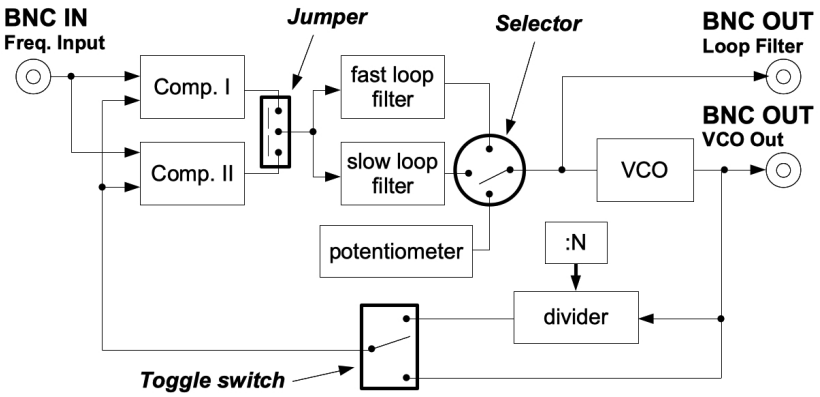


Figure 3.9: Block diagram of the circuit board for the laboratory exercise.

3.5.1 VCO voltage to frequency characteristic

Measurement set-up

1. selector in position ***Potentiometer*** (*Potenziometro*). In this circuit configuration the PLL feedback loop is open;
2. an oscilloscope (or a *multimeter*) is connected to the **Loop Filter** BNC connector. This test point allows to measure **VCO input voltage**;
3. an oscilloscope (or a *counter*) is connected to the **VCO Out** BNC connector, where **VCO output frequency** is measured.

By rotating the potentiometer knob, VCO voltage is varied from 0 to 9 V. Measurements of voltage and of the corresponding frequency have to be taken. About ten couples of values, suitably spaced along the voltage (abscissa) axis should suffice to trace a plot of the voltage to frequency characteristic with sufficient accuracy. If an oscilloscope is being used, it is suggested to make use of its **measurement functions**.

The minimum and maximum values, f_{min} and f_{MAX}, of the VCO output range[1] must also be measured, as they will be needed in the following parts of this exercise.

The VCO characteristic allows to determine the frequency range where the VCO input-output relationship can be considered approximately linear. Within this range, residual non-linearity can be assessed in different ways. A simple approach is provided in the IC *data-sheet*, where the following formulas are applied to compute a non-linearity index:

$$\text{non-linearity} = \frac{f_0 - f\left(\frac{1}{2}V_{DD}\right)}{f_0} \times 100 \quad [\%] \tag{3.3}$$

with:

$$f_0 = \frac{f\left(\frac{V_{DD}}{4}\right) + f\left(\frac{3V_{DD}}{4}\right)}{2}. \tag{3.4}$$

By the same criterion, the VCO constant K_O within its linear input-output range can be determined as:

$$K_O = \frac{f\left(\frac{3}{4}V_{DD}\right) - f\left(\frac{1}{4}V_{DD}\right)}{\frac{1}{2}V_{DD}} \quad [\text{Hz/V}]$$

3.5.2 PLL lock and capture ranges

NOTICE As described in Section 3.3, the circuit board allows multiple circuit configurations. It is possible to work using either *Phase Comparator I* or *Phase Comparator II*, and a choice of either fast or slow loop filter is provided.

A frequency divider may be included in the PLL fedback loop only when using *Phase Comparator II*.

Measurement set-up

1. selector in position ***Slow loop*** (*Anello lento*) or ***Fast loop*** (*Anello veloce*);
2. frequency divider OFF (orange LED must be off).
3. signal generator connected to the BNC input ***Freq. Input***;
4. measurement points:
   - one oscilloscope channel connected to the ***VCO Out*** BNC output;
   - one oscilloscope channel connected to the ***Loop Filter*** BNC output;
   - using a **'T' BNC connector**, the generator output can also be connected to another oscilloscope input channel.
5. a plot of the measured VCO voltage to frequency characteristic (see 3.5.1) should be available **before** measuring the lock and capture ranges.

[1] It is reminded that the output frequency range is determined through the choice of the values of external passive components C_1, R_1 and R_2.

IMPORTANT The circuit power supply inputs are $V_{DD} = +9$ V and $V_{SS} = 0$ and the phase comparator input is AC-coupled. This means PLL input voltage provided by the signal generator **should not exceed 9 V peak-to-peak**.

The IC employed in this exercise is a series 4000 CMOS component, whose input thresholds are: $v_{iLMAX} = 30\%V_{DD}$ and $v_{iHmin} = 70\%V_{DD}$. If these thresholds are not crossed some parts of the circuit, in particular *Phase comparator I*, might not be working correctly with some signals. In this case, it is suggested to set the PLL peak-to-peak input voltage to greater than $40\%V_{DD}$, that is, at least 3.6 V.

Measurement with Phase comparator I

The circuit configuration considered here assumes the use of

- *Phase Comparator I*. Ensure that the *jumper* is placed in the left (*Phase comparator I*) position;
- a **fast** loop filter.

Slight modifications may be needed for other PLL circuit configurations, the most significant differences are noted in the following.

Free-running frequency

Temporarily disconnect the generator from the BNC input ***Freq. Input*** to measure the PLL *free-running frequency* that should have settled to an intermediate value between f_{min} ed f_{MAX}. The behavior of the VCO control voltage is presented by the oscilloscope trace relating to the **Loop Filter** BNC output. Its mean value is expected to be close to $V_{DD}/2$. A superposed ripple at the same frequency as the VCO output shows the effect of low-pass filtering of the *Phase comparator I* output that, without a reference PLL input, generates a square wave with 50% duty cycle.

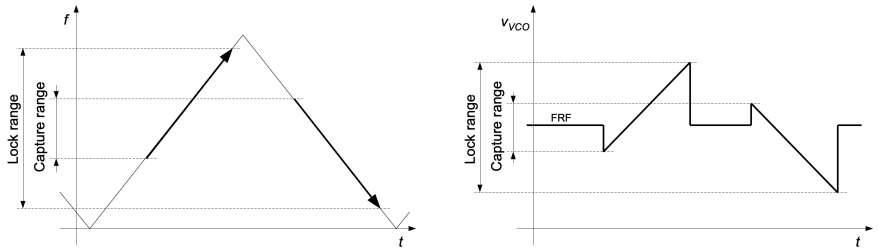
Using a frequency-modulated input

Measurement of the PLL lock and capture ranges with *Phase comparator I* requires a gradual, slow change of the input frequency. One way to approach this measurement is shown Fig. 3.10a: the generator waveform is frequency-modulated by a **triangle wave** so that its frequency varies, *slowly and steadily*, from $f_{low} < f_{min}$ to $f_{high} > f_{MAX}$ and back.

During the upward ramp of the triangle wave, frequency is progressively increased until the **lower limit of the capture range** in reached, at which point $f_{out} = f_{in}$. The input frequency is then tracked until the **upper limit of the lock range** is reached, after which the PLL output returns to the FRF. During the downward slope instead, the higher limit of the capture range is reached first, lock is achieved and retained until the lower limit of the lock range is reached[2].

The corresponding behavior of the VCO control voltage, that can be measured at the ***Loop Filter*** BNC output, is represented in Fig. 3.10b. The

[2]**N.B.**: *Phase comparator I* may occasionally cause the PLL to lock onto harmonics of the input fundamental frequencies. This should be regarded as an not guaranteed occurrence.



(a) input frequency; (b) loop filter output.

Figure 3.10: Scan of PLL input frequencies and limits of lock and capture ranges.

resulting trace displayed by the oscilloscope allows to determine the voltage values corresponding to the limits of both lock range and capture range by means of cursors. Using the plot of the measured VCO voltage to frequency characteristic, these can be translated back to the desired frequency values.

Generator set-up

When setting the waveform generator for frequency modulation it should be remembered that:

- the **amplitude** setting refers to the unmodulated signal (that is not changed by FM modulation), that is called the **carrier**;
- the **frequency** setting refers to the unmodulated carrier signal and will be indicated in the following with f_C;
- the **waveform** setting refers to the shape of the unmodulated carrier signal;
- the **modulation amplitude** for FM is the maximum frequency deviation given in Hz and will be indicated in the following with F. The frequency-modulated signal will vary its fundamental frequency between $f_C - F$ and $f_C + F$;
- the **modulation frequency** setting, indicated in the following with f_m, determines how many times per second the generated signal frequency will cycle from its minimum to maximum value and back;
- the **modulation waveform** setting determines how signal frequency will vary over time.

Setting up a Keysight 33600 waveform generator for this measurement requires the following steps:

- **Carrier waveform**
  - using the **Waveform** key, select the generation of a square wave (a sinewave, or any other waveform are also possible choices – in these cases, check first that the PLL is able to lock on the selected waveform);

  - using the **Parameters** menu, select frequency value:

$$f_C = \frac{f_{high} + f_{low}}{2}$$

    where $f_{low} < f_{min}$ and $f_{high} > f_{MAX}$, as noted above;
  - check that waveform amplitude is set correctly.

- **Modulating waveform**
  - select the option **Type** from the **Modulation** menu; set the type to **FM**;
  - set **Shape** to triangular in the modulating waveform configuration menu;
  - set modulation amplitude ΔF (**FM Ampl**), remembering that its value **is in Hz for FM**:

$$\Delta F = \frac{f_{high} - f_{low}}{2};$$

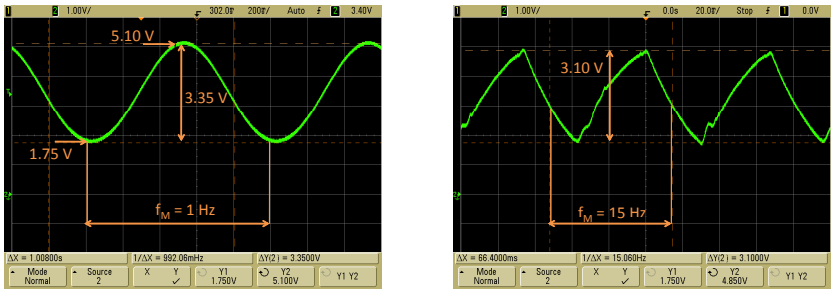
  - provide a suitable value for modulation frequency (**FM Freq**). Remember a **slow** frequency variation is required, more specifically, to ensure that the VCO control voltage correctly follows the modulating triangle waveform this should fall well within the loop filter bandwidth. As a rule of thumb, f_m might be set to $\frac{1}{10}$ of the loop filter bandwidth (see below);
  - set (**Modulate − On**).

Choice of the modulation frequency – IMPORTANT

When the PLL test input is a frequency-modulated signal, the shape of the modulating waveform should be reproduced by the shape of the VCO control voltage.

Modulation amplitude indicated by the waveform generator (in Hz for FM) can be compared with voltage at the loop filter output, for instance Fig. 3.11a presents the measured loop filter output when the PLL input is a FM signal with a sinusoidal modulating waveform at frequency $f_m = 1$ Hz. Peak-to-peak amplitude of $v_O(t)$ corresponds to twice the modulation amplitude, with carrier frequency f_C. If the measured VCO constant is $K_O = 3000$ Hz/V, the measured peak-to-peak voltage $\Delta V = 3.35$V corresponds to variation over a frequency interval of 10.05 kHz (thus, modulation amplitude is about ±5 kHz).

To prevent distortion at the loop filter output, it is essential that the frequency spectrum of the modulation waveform remains within the filter bandwidth. For the PLL considered in Fig. 3.11a, if modulation frequency is increased to $f_m = 15$ Hz while modulation amplitude and waveform remain the same, the measured loop filter output is shown in Fig. 3.11b. Non-linear distortion is partly due to attenuation by the loop filter and partly to the PLL tracking the input signal in a different way. Proportionality to the modulating waveform is thus lost.



(a) FM with 1-Hz sinusoidal modulation (b) FM with 15-Hz sinusoidal modulation

Figure 3.11: Effect of loop filter bandwidth limitation on VCO control voltage. Non-linear distortion occurs in this case.

Measurement with Phase comparator II

With the *jumper* now placed in the right (*Phase comparator II*) position, temporarily disconnect the generator from BNC input ***Freq. Input***. In this case the VCO control voltage is close to zero and the PLL *free-running frequency* that should approximately coincide with f_{min}.

Set up the waveform generator as before and repeat the observation. Starting from f_{min}, the PLL will be able to lock to any frequency, up to an upper limit close to f_{MAX}. By measuring the *loop filter* output it can be verified that the VCO control voltage varies in accordance with the VCO transfer characteristic measured previously. In this case, since the PLL feedback loop is closed the voltage range might differ slightly.