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Phase Locked Loop (PLL)

Lecture #9
Electronic measurements
Alessandro Pozzebon

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Analysis of complex devices

- Analysing a complex device:
  - **Characterization**
  - **Diagnostic**

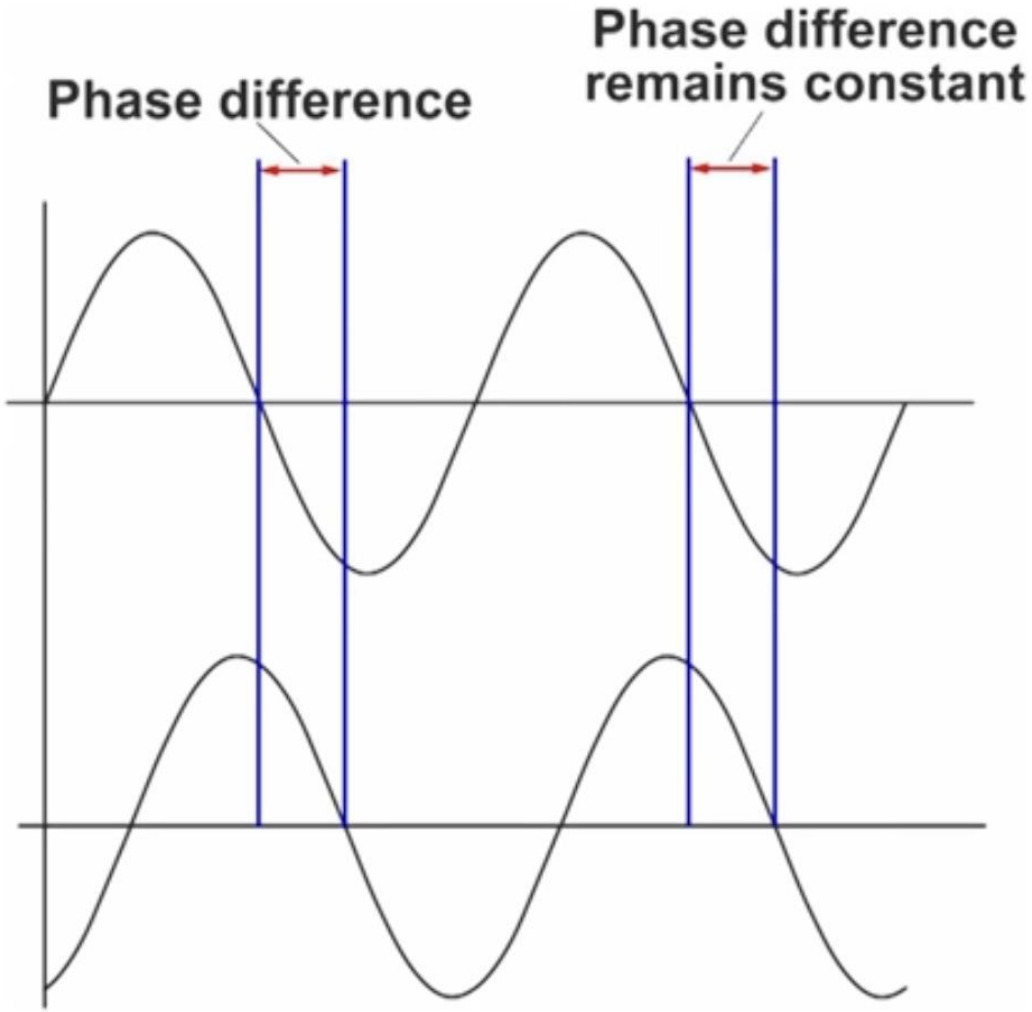
- **Understand device operating principles** to establish the expected behaviour, based on which deviations leading to possible malfunctions can be evidenced
- **Define suitable test points and execute measurements** to determine the actual device behaviour
- **Determine the dependability of test indications** by analyzing features and performances of measuring instrumentation

The Phase Locked Loop (PLL)

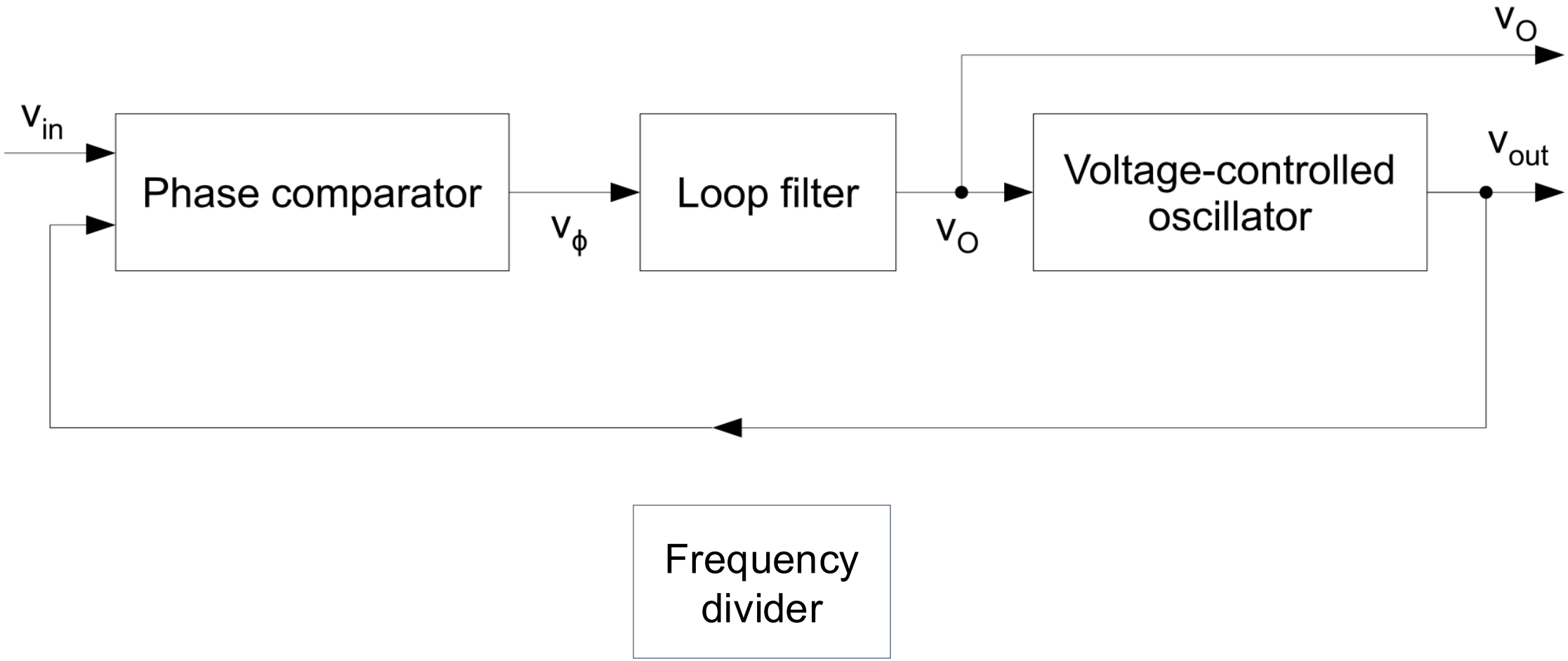
- **Feedback system** that tracks a periodic input and produces an output signal having the same fundamental frequency

- **Applications**:
  - Frequency synthesizers
  - Clock generators
  - FM or FSK demodulators
  - Clock recovery circuits

The Phase Locked Loop (PLL)



PLL: operating principle



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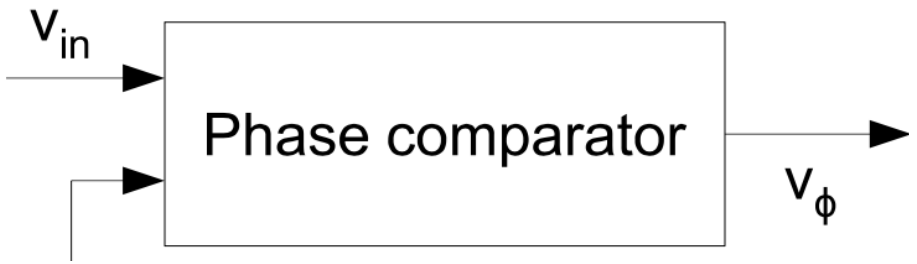
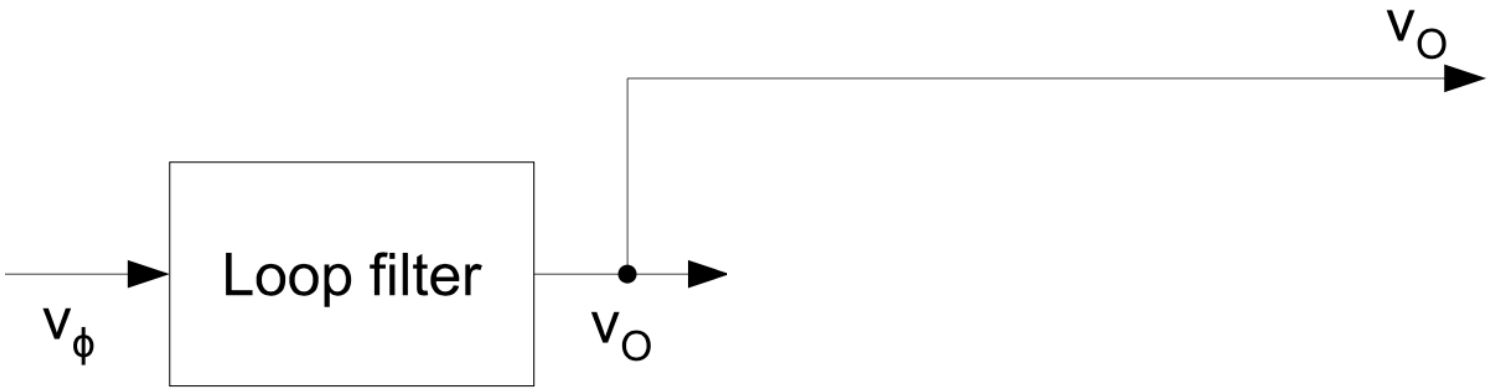


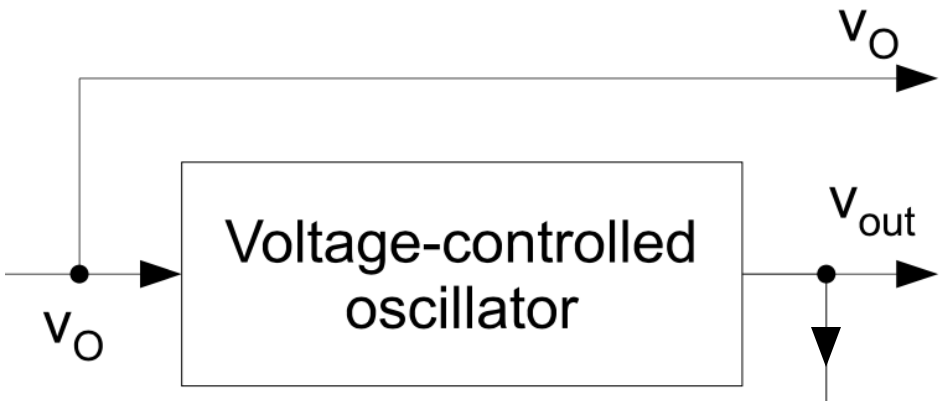
- **Phase comparator:** compares the instantaneous phase of the input signal $v_{in}(t)$ with the instantaneous phase of the signal $v_{out}(t)$ generated within the PLL by the voltage-controlled oscillator
- The **phase comparator output** is a voltage signal $v_{\varphi}(t)$, whose mean value is proportional to the phase difference between the two inputs

PLL: operating principle



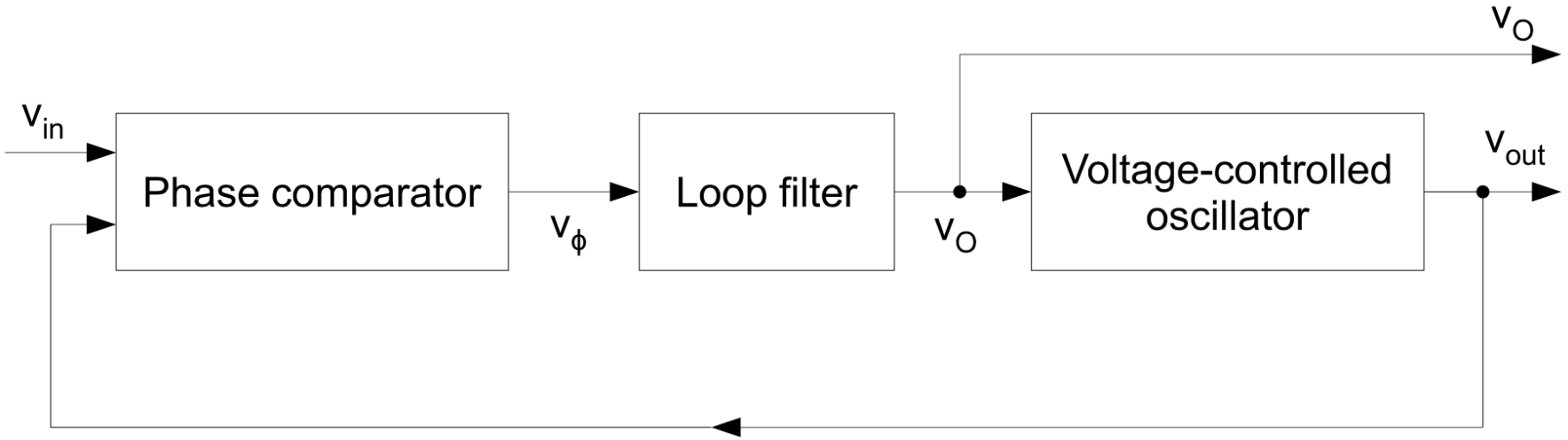
- **Loop filter:** has a low-pass frequency response, and its output is the mean value of $v_\varphi(t)$

PLL: operating principle



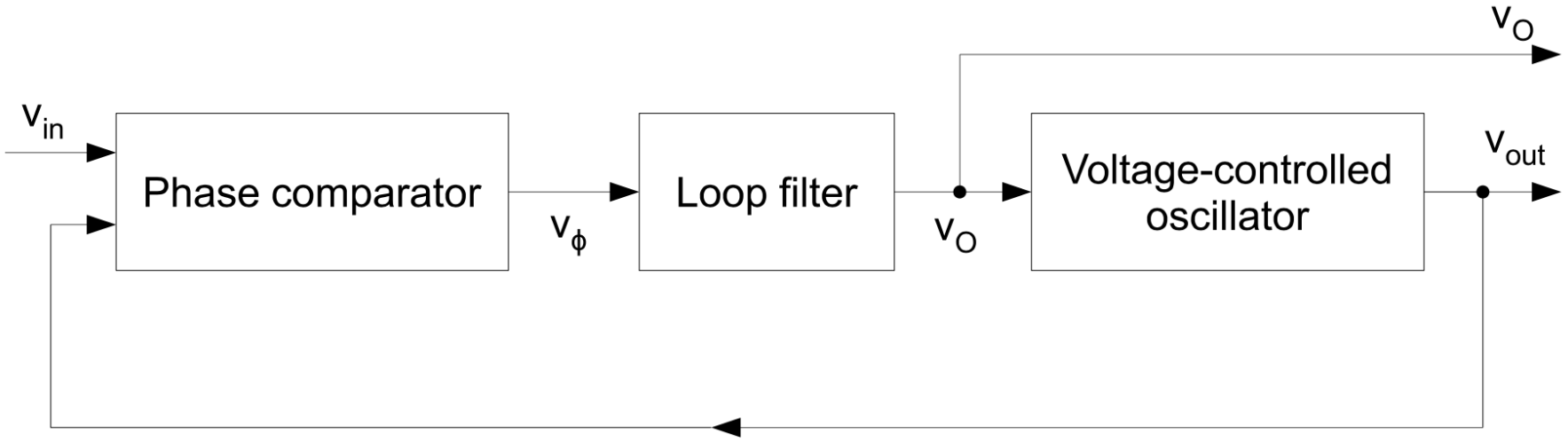
- **Voltage Controlled Oscillator (VCO):** produces a periodic signal whose fundamental frequency is proportional to the value of the input voltage
- The loop filter output voltage $v_o(t)$ is employed as the **VCO control voltage**

PLL: operating principle



- **Sinusoidal signals**
- $f_{in} \neq f_{out}$
- Their phase difference will **vary with time**
- VCO input $v_O(t)$ is **proportional to the difference of frequency and instantaneous phase** between $v_{in}(t)$ and $v_{out}(t)$

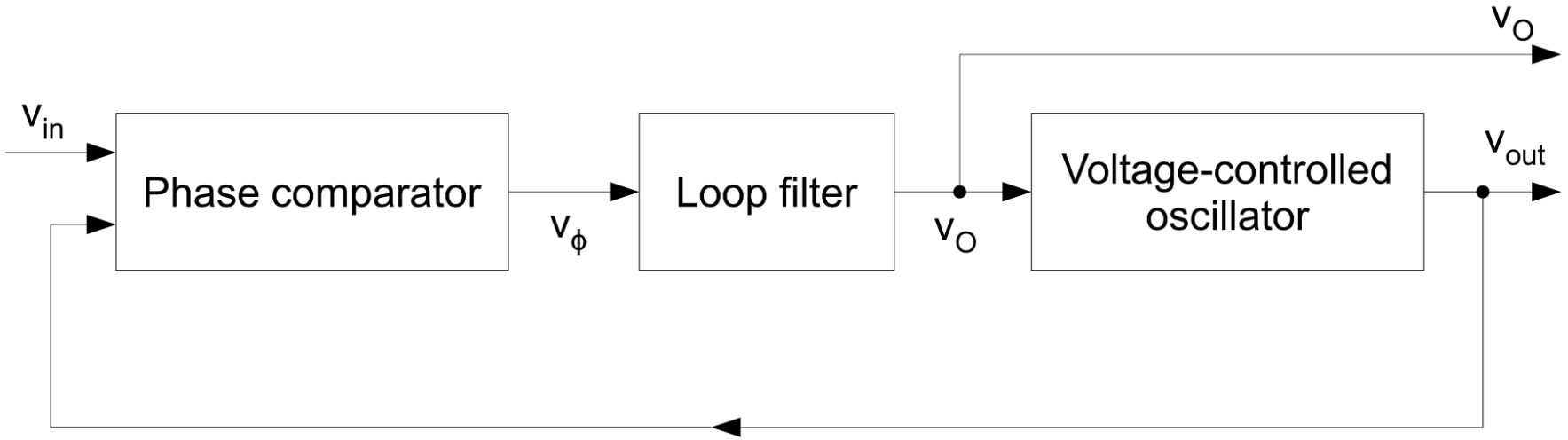
PLL: operating principle



- $v_{in}(t) = Asin(2\pi f_{in}t + \phi_{in})$
- $v_{out}(t) = Asin(2\pi f_{out}t + \phi_{out})$

- $\Delta\phi(t) = [2\pi(f_{out} - f_{in})t + \phi_{out} - \phi_{in}]_{mod(2\pi)}$
- Periodic quantity with period 2π radians
- $\Delta\phi(t)$ increases if $f_{out} > f_{in}$ and decreases if $f_{out} < f_{in}$

PLL: operating principle

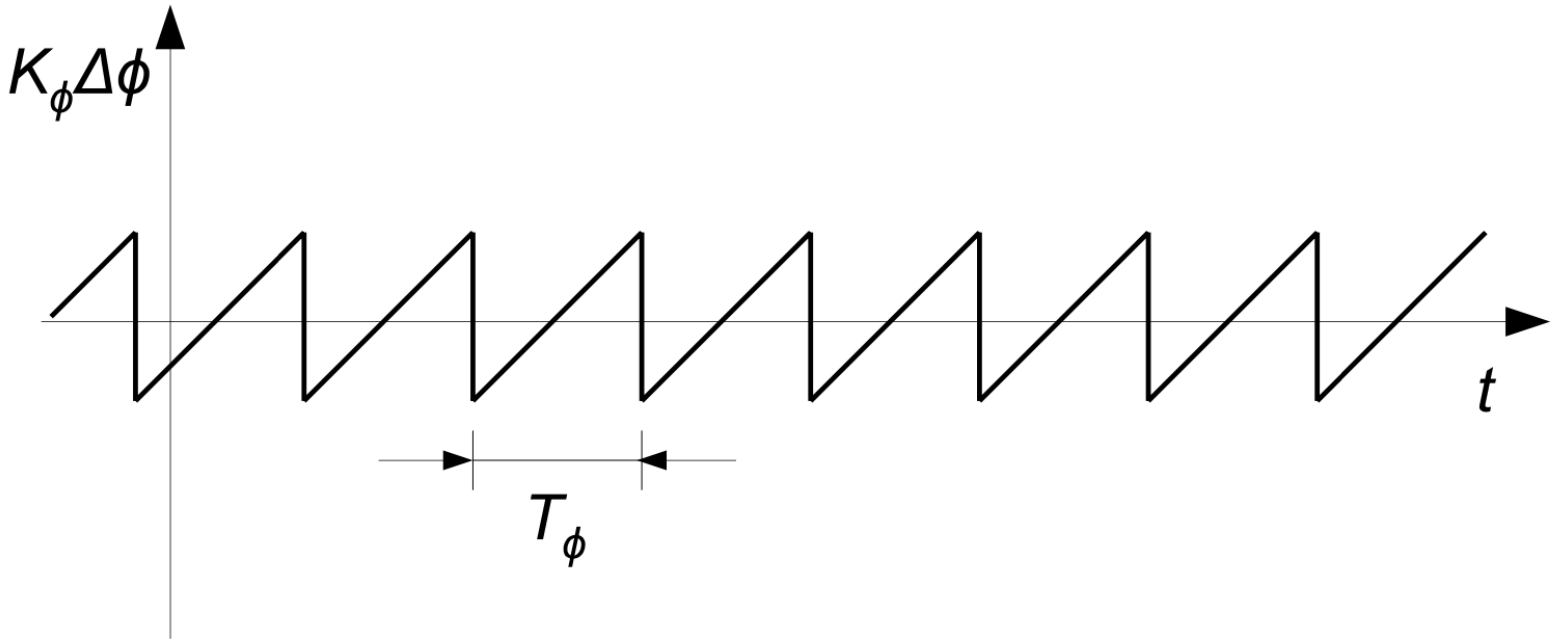


- Phase comparator relationship:

$$v_\varphi(t) = K_\phi \cdot \Delta\phi(t) \quad \text{with} \quad |\Delta\phi(t)| < \pi$$

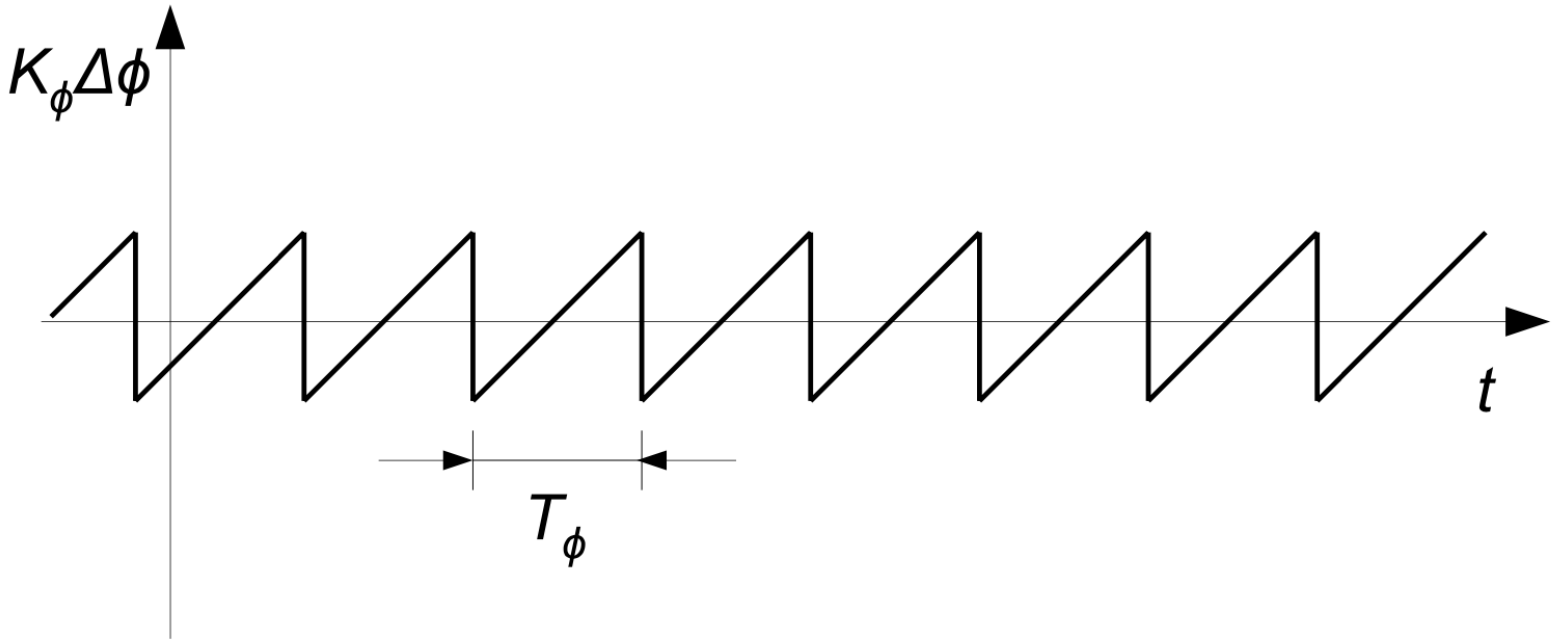
- K_ϕ is given in [V/rad]
- **Sawtooth waveform** with period $T_\phi = [1/(f_{out} - f_{in})]$

Free Running Frequency



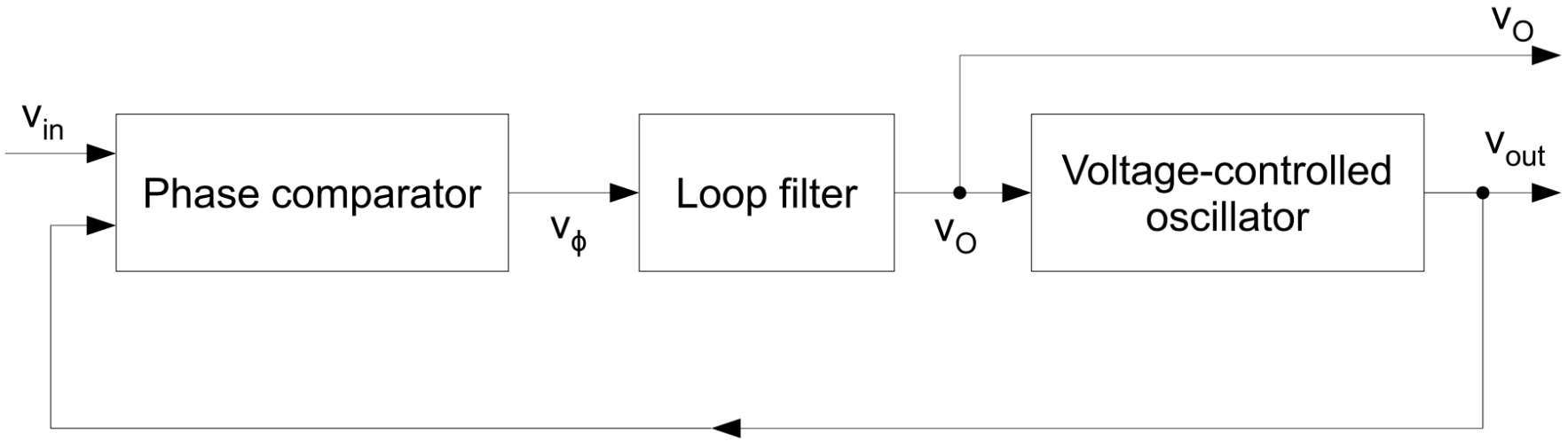
- As long as the difference between the two frequencies remains constant, the phase comparator output voltage varies **linearly** within its range with period T_ϕ
- This condition occurs when no signal is present at the PLL input
- **Free Running Frequency (FRF)**

Free Running Frequency



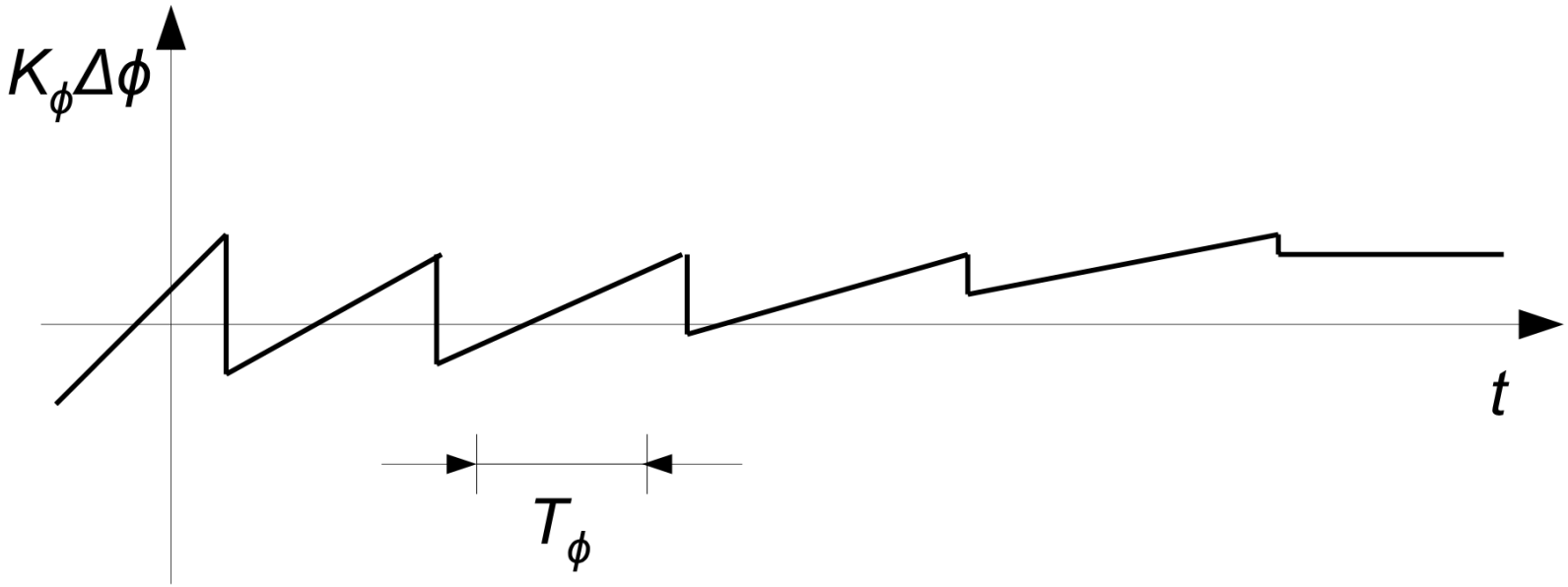
- FRF value is determined by the **characteristics of all PLL building blocks**, particularly by the behaviour of the **loop filter**
- When **lock to the input frequency is lost**, the PLL also settles into a similar condition

Lock Phase



- As VCO control voltage varies, the **feedback** in the system should tend to **reduce the difference** between the output and the input frequencies
- When f_{out} is close enough to f_{in} the VCO gets "**locked**" onto it
- In the lock phase, if the input frequency remains constant, the phase comparator output is expected to **remain constant**

Lock Phase



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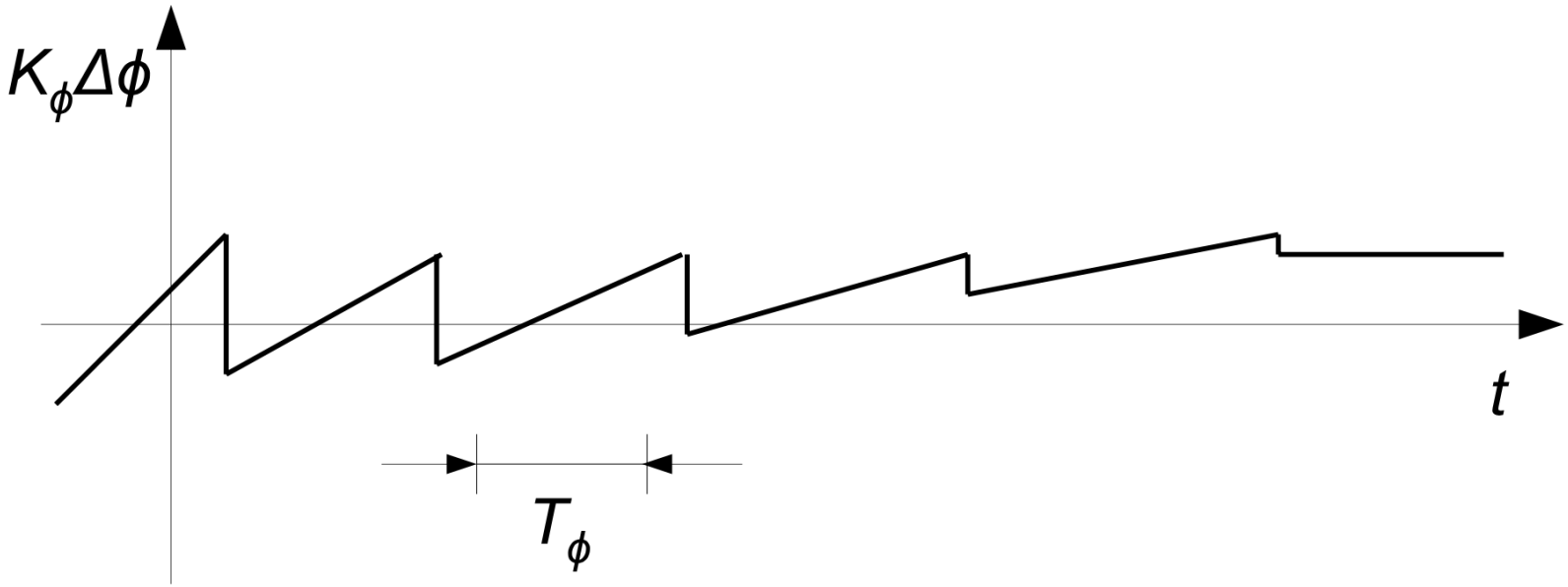
Lock Phase



- The final **steady state voltage** corresponds to the control input at which the VCO produces the **desired frequency**
- If the VCO **input voltage range and the phase comparator output range coincide**, the PLL might be able to lock to the input signal over the whole VCO frequency interval

Lock range and capture range

- The actual interval may be **narrower** and depends on the features of the loop filter
- **Two different interval de**finitions need then to be considered

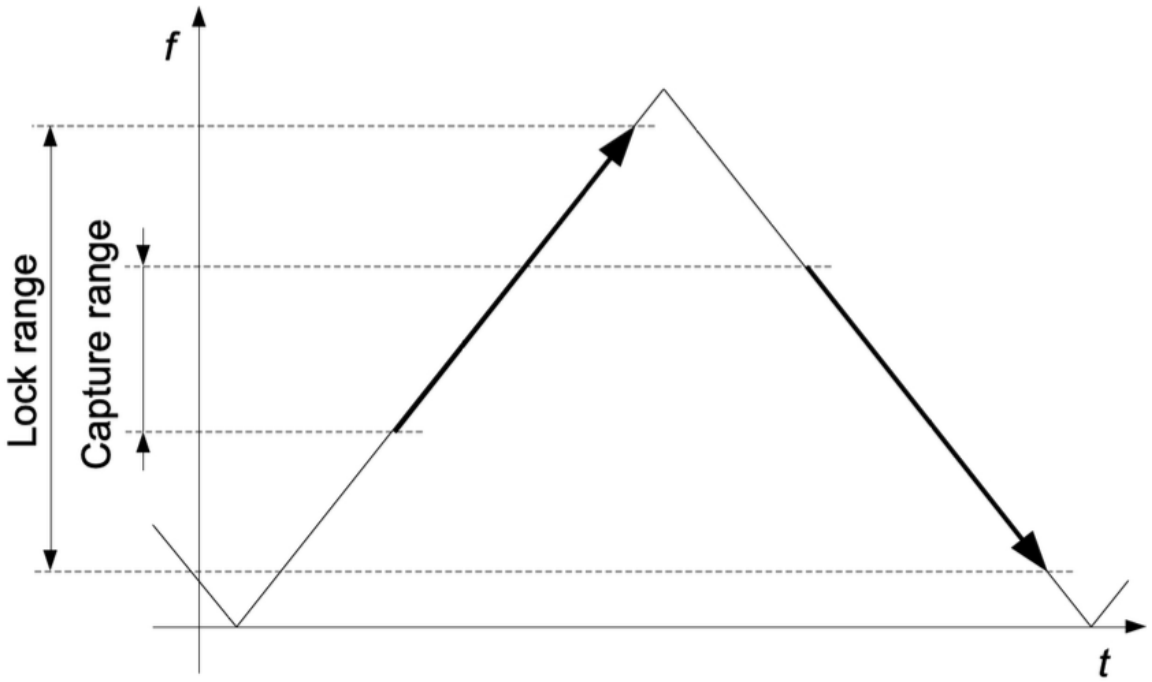
- **LOCK RANGE:**
- The PLL can track the input frequency variations as long as they remain **within a certain interval**
- **FM demodulator**: variable voltage, proportional to the input frequency, at the loop filter output

Lock range and capture range

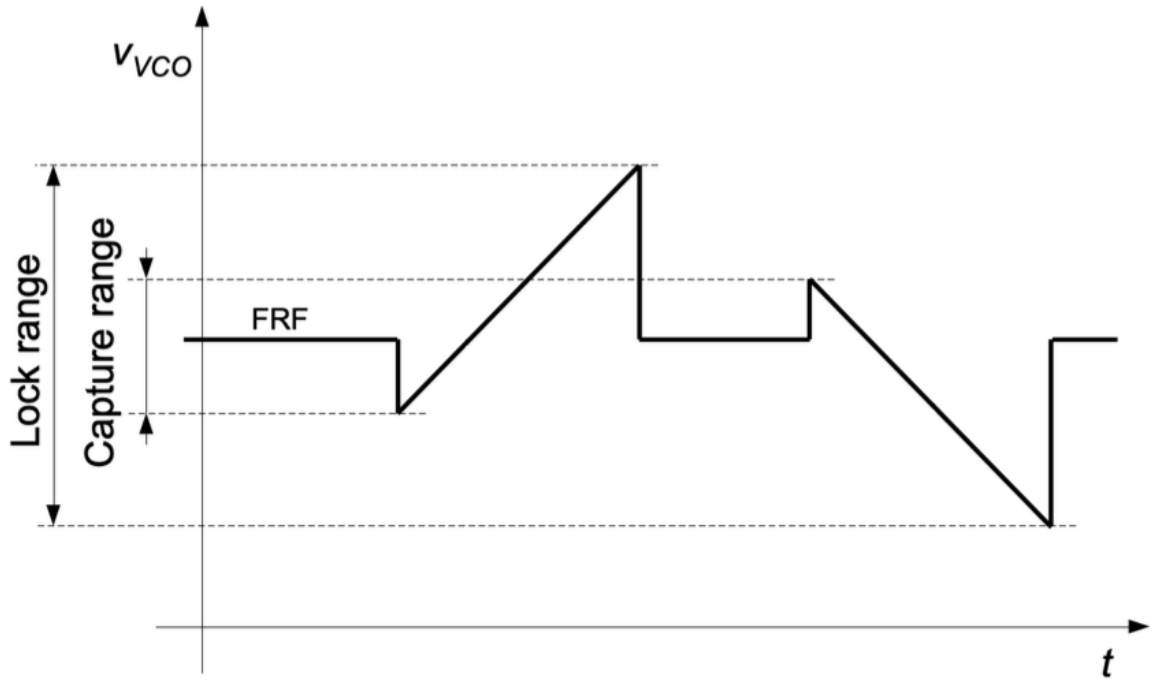
- The actual interval may be **narrower** and depends on the features of the loop filter
- Two different interval definitions need then to be considered

- **CAPTURE RANGE:**
- The PLL can lock onto the input frequency and track it, starting from a VCO free-running state
- This condition is **more demanding** compared to the lock range
- Capture range is determined by phase comparator and loop filter characteristics

Lock range and capture range



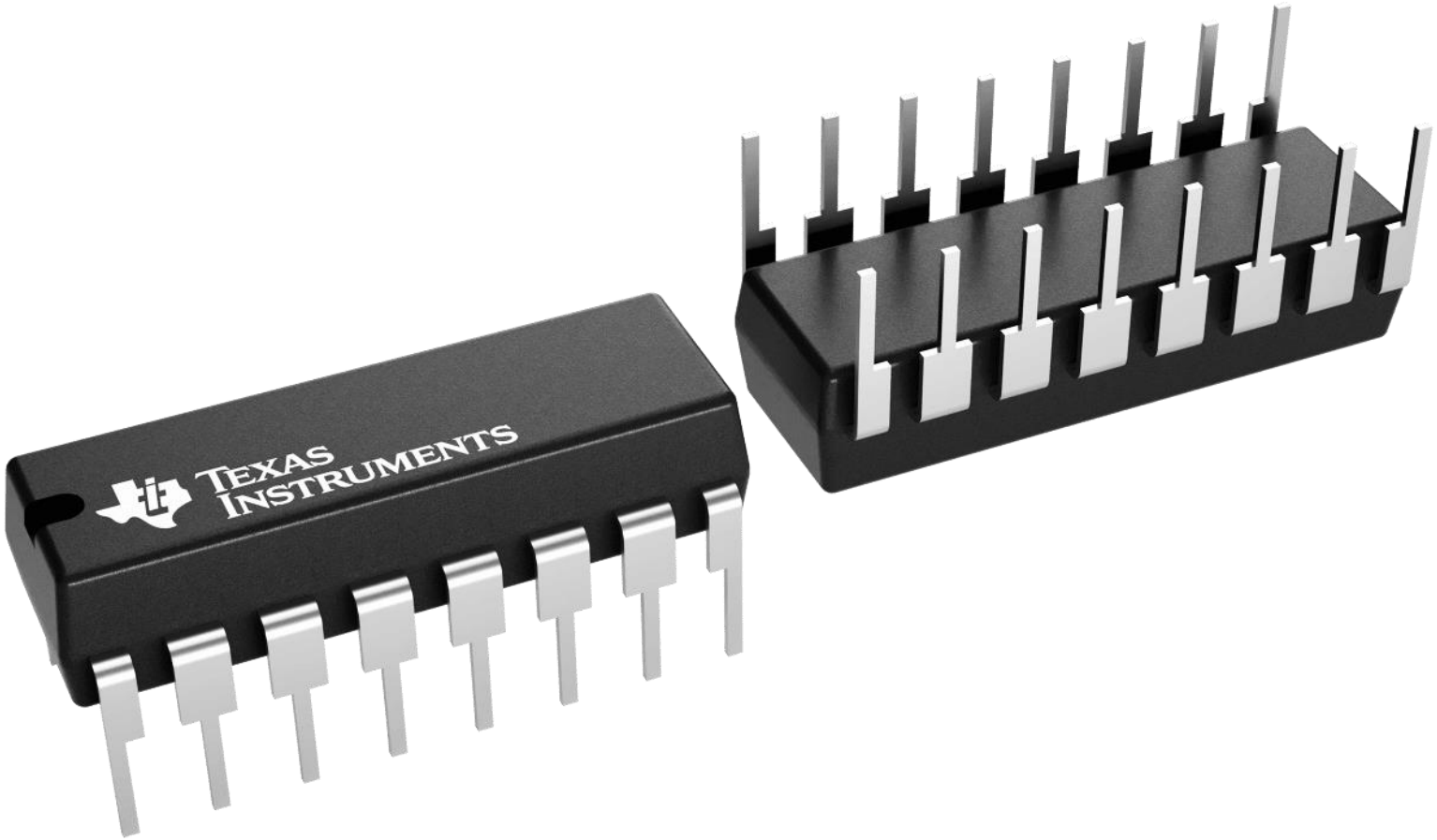
input frequency



loop filter output

Measured device

CD4046B



Measured device

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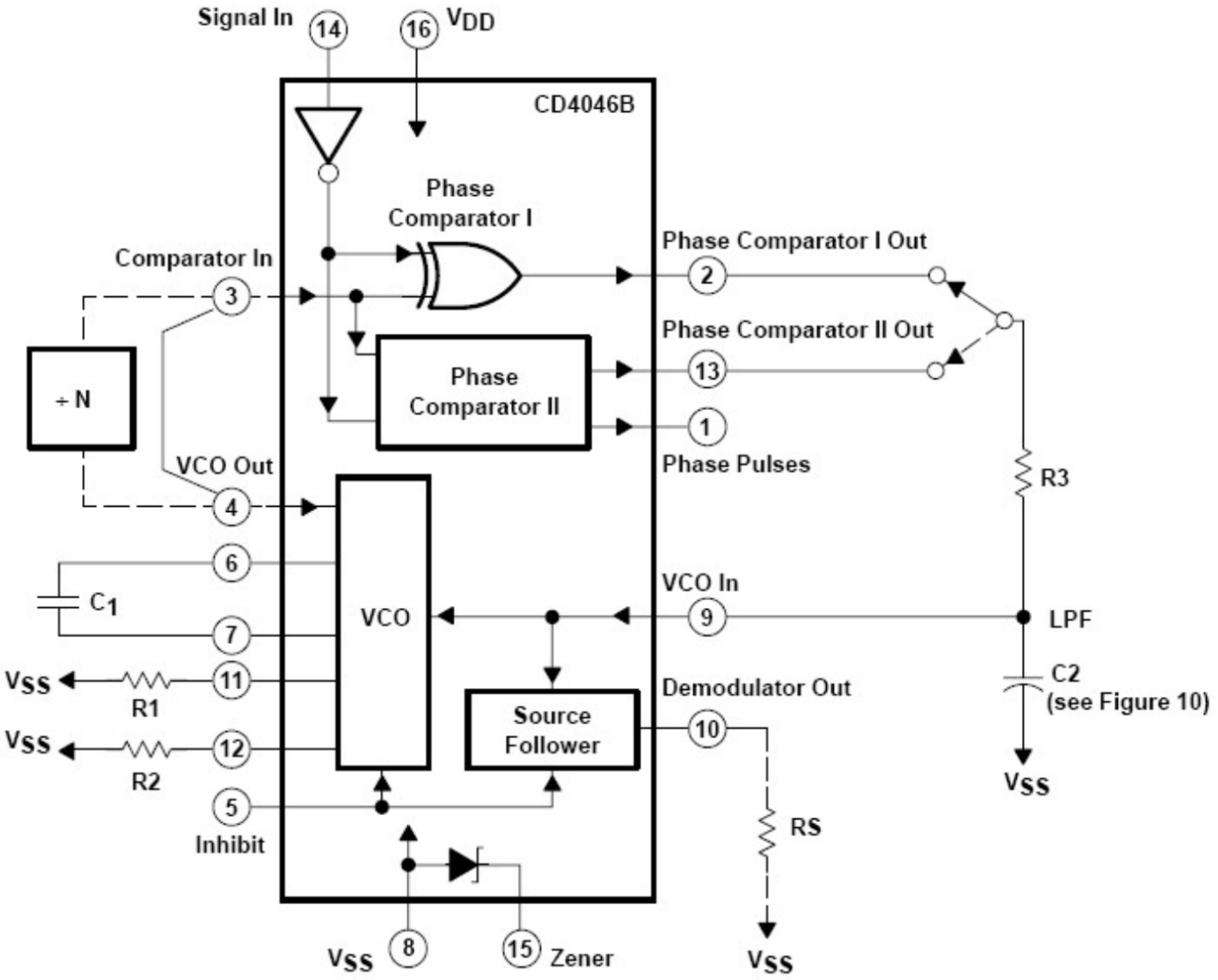

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Voltage Controlled Oscillator

- **Square wave oscillator** realized by feedback-connected logic inverters
- The **output frequency range** is set with an external resistor and an external capacitor (R_1 and C_1 in the scheme)
- Circuit power supply voltage V_{DD}, with $V_{SS} = 0$.
- VCO control voltage between 0 and V_{DD} ⇒ smaller useful range

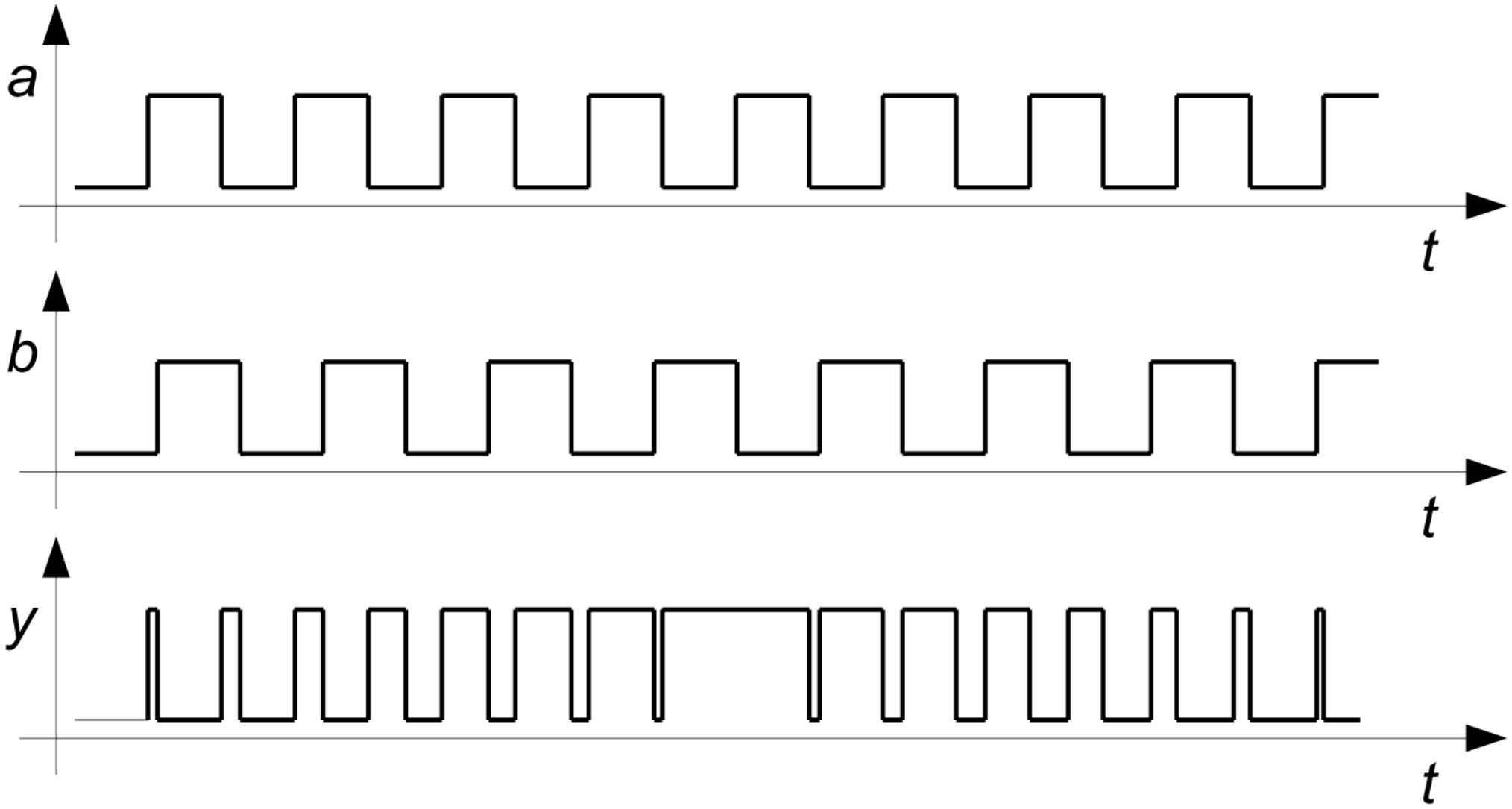
- **Loop Filter** realized with passive components R_3 and C_2

Phase Comparator I

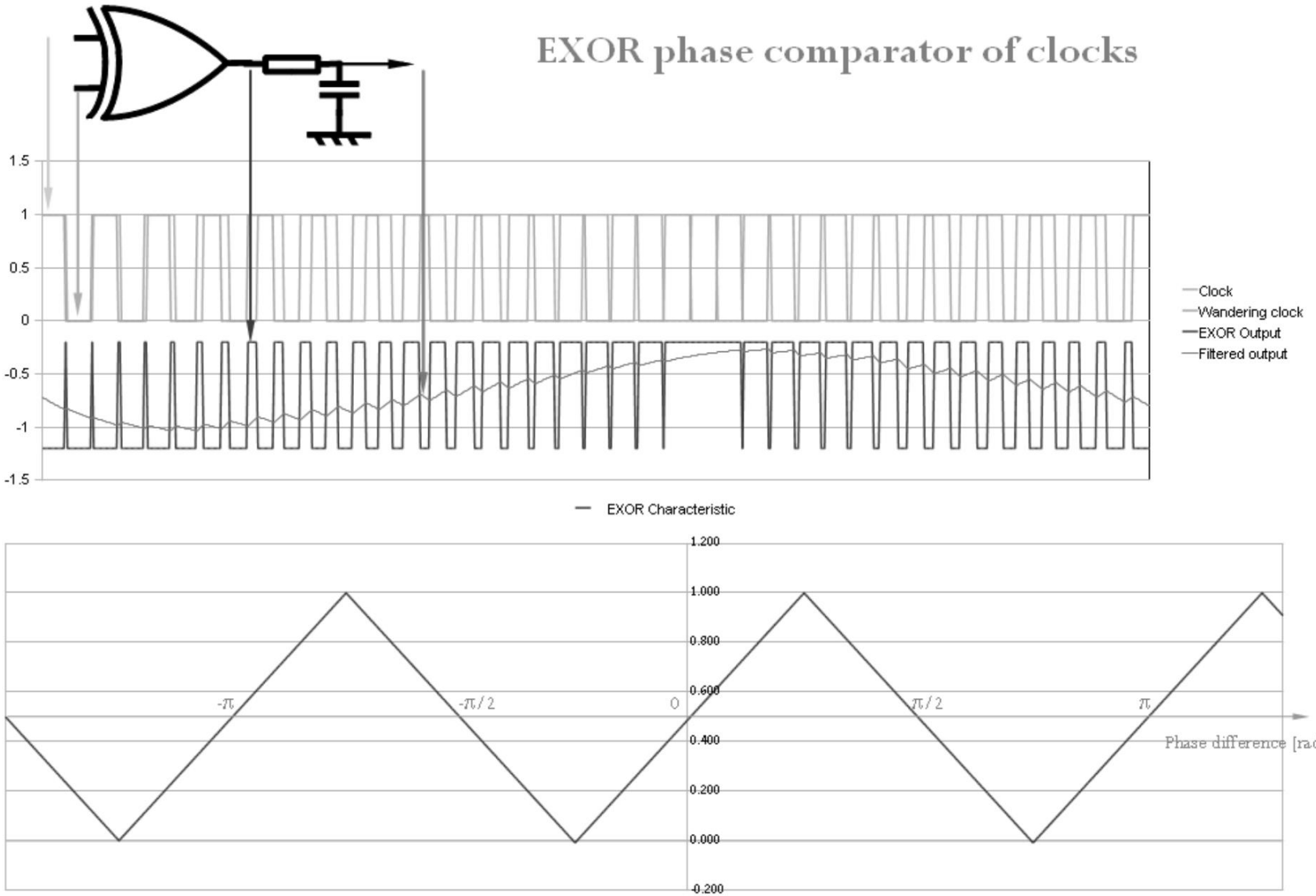
- **Exclusive-OR (XOR) logic gate**
- The output is a sort of "**product**" between the two signals
- If the two inputs are at the **same frequency**, the XOR gate output is a square wave at the same frequency, having a duty cycle proportional to the phase shift between them
- If the two inputs are at **different frequencies**, f_{in} and f_{VCO}, the XOR gate output is a square wave whose duty-cycle varies at frequency $|f_{in} - f_{VCO}|$

a	b	y
0	0	0
0	1	1
1	0	1
1	1	0

Phase Comparator I



Phase Comparator I



Phase Comparator I

- If **no signal** is present at the PLL input, or when the circuit is out of lock, the mean voltage at the output of Phase comparator I is $\mathbf{V_{DD}/2}$
- The VCO output will correspond to this voltage input, that determines the PLL **free-running frequency**
- When the PLL has **locked** to the input, the phase shift of the VCO output is **constant** and depends on the generated signal frequency

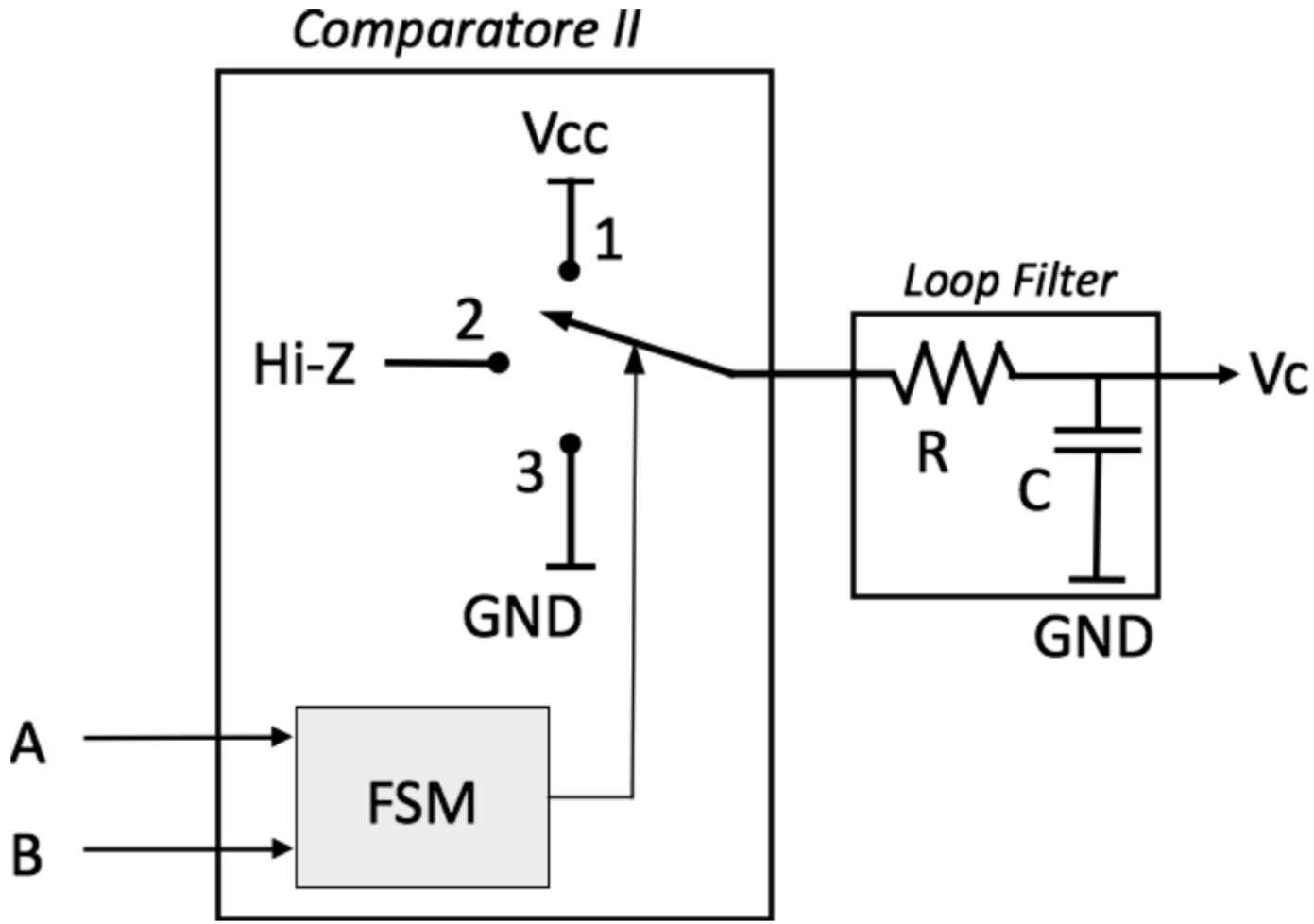
Phase Comparator I

- **ADVANTAGES**
  - Simplicity
- **DISADVANTAGES**
  - The loop filter output tends to be affected by **ripple** ⇒ Possible problem for stability
  - The XOR gate output varies its duty cycle at a frequency $|f_{in} - f_{VCO}|$. If the PLL is out of lock and the difference $|f_{in} - f_{VCO}|$ is beyond the loop filter bandwidth, the PLL will not be able to lock on the input

- "**capture**" is possible as long as the input frequency is not too far from FRF
- Once lock has been achieved, however, the input frequency can vary over a **much wider range**

Phase Comparator II

- **Sequential digital logic** network that realizes a Finite State Machine
- State changes are triggered exclusively by **rising edge** detection on the input signals and determine the transitions of a three-state output
- The output is connected to an **RC electrical network** as the PLL loop filter



Phase Comparator II

- The FSM controls the position of a **three-way switch**, enabling one of three possible outputs:
  - **Power supply voltage V_{DD}** (1 – logic output 'high' logic state): in this case, capacitance C is charged through resistance R
  - **Floating high impedance output** (2 – logic output in 'high-Z' state): capacitance charge remains unchanged
  - **Ground** (3 – logic output 'low' logic state), in this case, capacitance C is discharged through resistance R

Phase Comparator II

- **State transitions** in the FSM take place according to the following rules:
  - if a rising edge is detected on **input 'A'** (to which the reference input signal is connected), the state of the switch must be increased by 1
  - if a rising edge is detected on **input 'B'** (to which the feedback signal from the VCO is connected), the state of the switch must be decreased by 1

- The two operations correspond, respectively, to **increasing or decreasing** the VCO output frequency
- When the PLL is in a constant-frequency lock condition, the phase comparator output should ideally remain in the **high-impedance** state most of the time
- Charge in the loop filter capacitance then changes little, since the VCO input impedance is also high

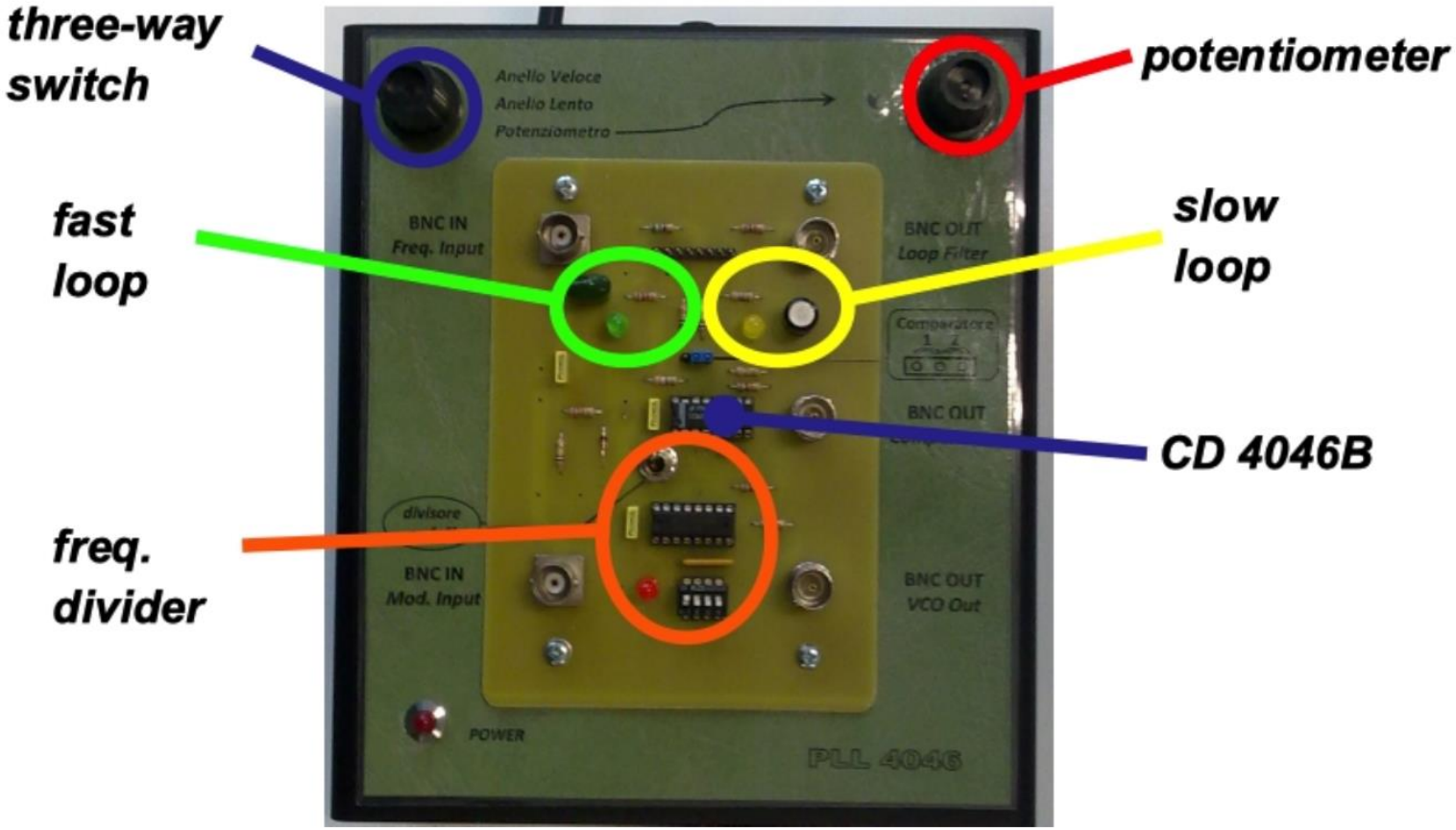
Phase Comparator II

- The edges of the two phase comparator inputs happen to be **nearly simultaneous**, which results in a continuous sequence of near-instant corrections

- **ADVANTAGES**
  - This avoids capacitance self-discharge
- **DISADVANTAGES**
  - This causes slight perturbations that translate into small variations of the VCO output frequency

- Capture range and lock range about coincide
- FRF is at lower end of the PLL operating range

The laboratory board



VCO voltage to frequency characteristic

Measurement set-up

1. Selector in position **Potentiometer** (Potenziometro). In this circuit configuration the PLL feedback loop is open
2. **Oscilloscope** (or multimeter) connected to the **Loop Filter BNC** connector. This test point allows to measure **VCO input voltage**
3. **Oscilloscope** (or counter) connected to the **VCO Out BNC** connector, where **VCO output frequency** is measured

- **Potentiometer** knob rotation → VCO voltage variation from 0 to 9 V
- About 10 couples of values

VCO voltage to frequency characteristic

- f_{min} minimum VCO output frequency
- f_{MAX} maximum VCO output frequency

- VCO input-output relationship → Approximately linear
- Residual non-linearity

$$\text{non linearity} = \frac{f_0 - f\left(\frac{1}{2}V_{DD}\right)}{f_0} \times 100 \quad [\%]$$

where

$$f_0 = \frac{f\left(\frac{V_{DD}}{4}\right) + f\left(\frac{3V_{DD}}{4}\right)}{2}$$

VCO voltage to frequency characteristic

- f_{min} minimum VCO output frequency
- f_{MAX} maximum VCO output frequency

- VCO constant K_O

$$K_O = \frac{f\left(\frac{3V_{DD}}{4}\right) - f\left(\frac{V_{DD}}{4}\right)}{\frac{1}{2}V_{DD}} \quad [\mathrm{Hz/V}]$$

PLL lock and capture ranges

Measurement set-up

1. Selector in position **Slow loop** (Anello lento) or **Fast loop** (Anello veloce)
2. Frequency divider **OFF** (orange LED must be off)
3. **Signal generator** connected to the **BNC input Freq. Input**
4. Measurement points:
   - One oscilloscope channel connected to the **VCO Out BNC output**
   - One oscilloscope channel connected to the **Loop Filter BNC output**
   - Using a 'T' BNC connector, the generator output can also be connected to **another oscilloscope input channel**

A plot of the measured VCO voltage to frequency characteristic should be available before measuring the lock and capture ranges.

PLL lock and capture ranges

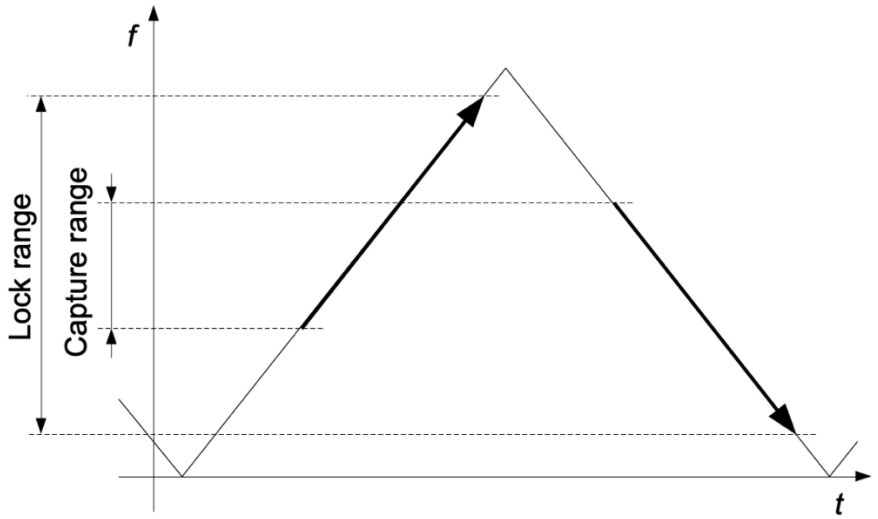
Phase comparator 1

- Phase Comparator I. Ensure that the jumper is placed in the left (Phase comparator I) position
- Fast loop filter

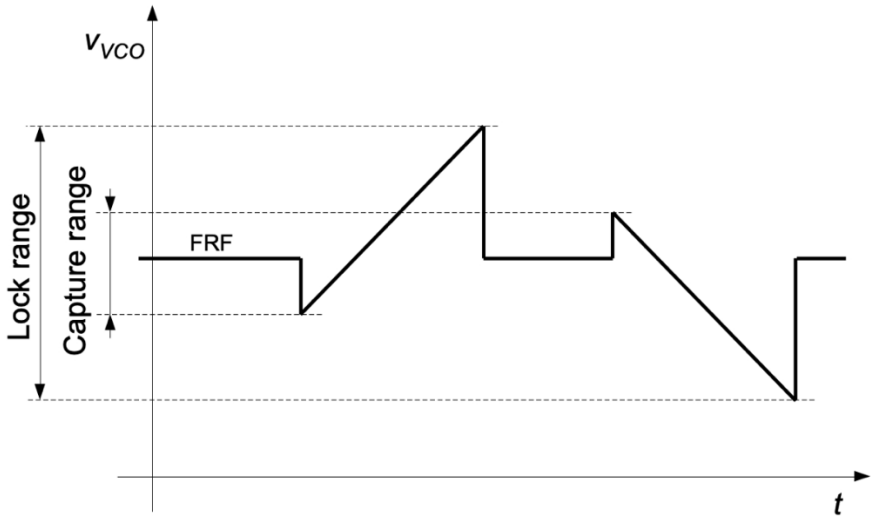
- **Free-running frequency**
  - Loop Filter BNC output close to $V_{DD}/2$
  - Superposed ripple at the same frequency as the VCO output → effect of low-pass filtering of the Phase comparator I output that, without a reference PLL input, generates a square wave with 50% duty cycle

PLL lock and capture ranges

- **Using a frequency-modulated input**
  - Gradual, slow change of the input frequency
  - Generator waveform frequency-modulated by a triangle wave so that its frequency varies, slowly and steadily, from $f_{low} < f_{min}$ to $f_{high} > f_{MAX}$ and back



(a) input frequency;



(b) loop filter output.

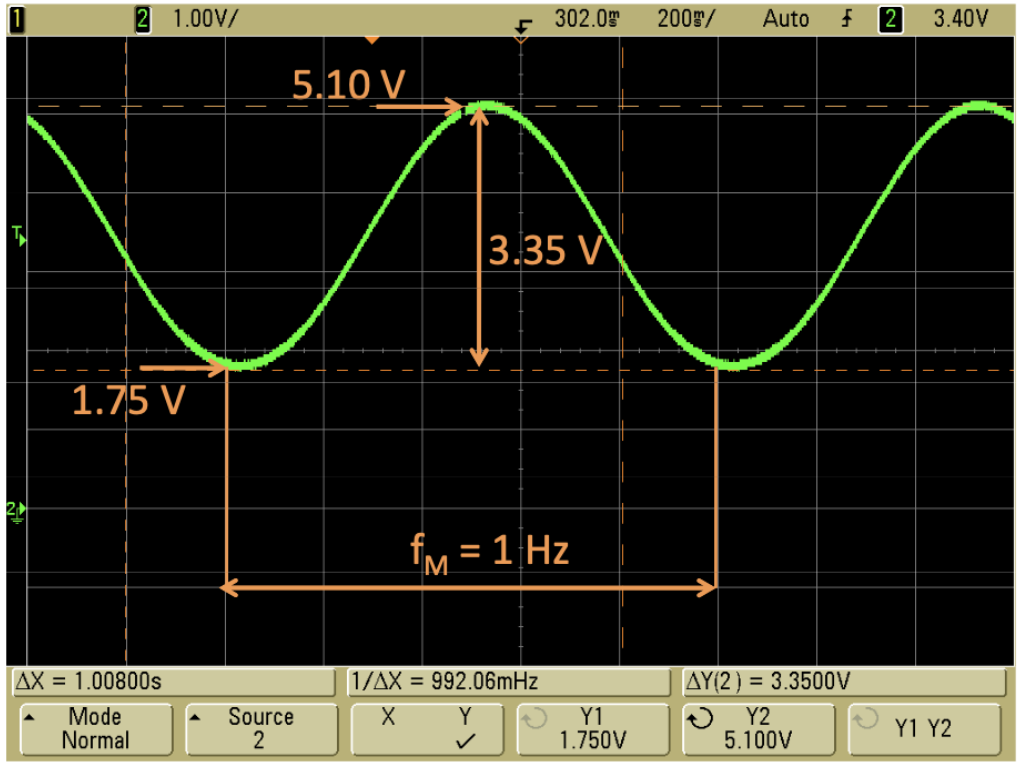
PLL lock and capture ranges

- **Generator set-up**

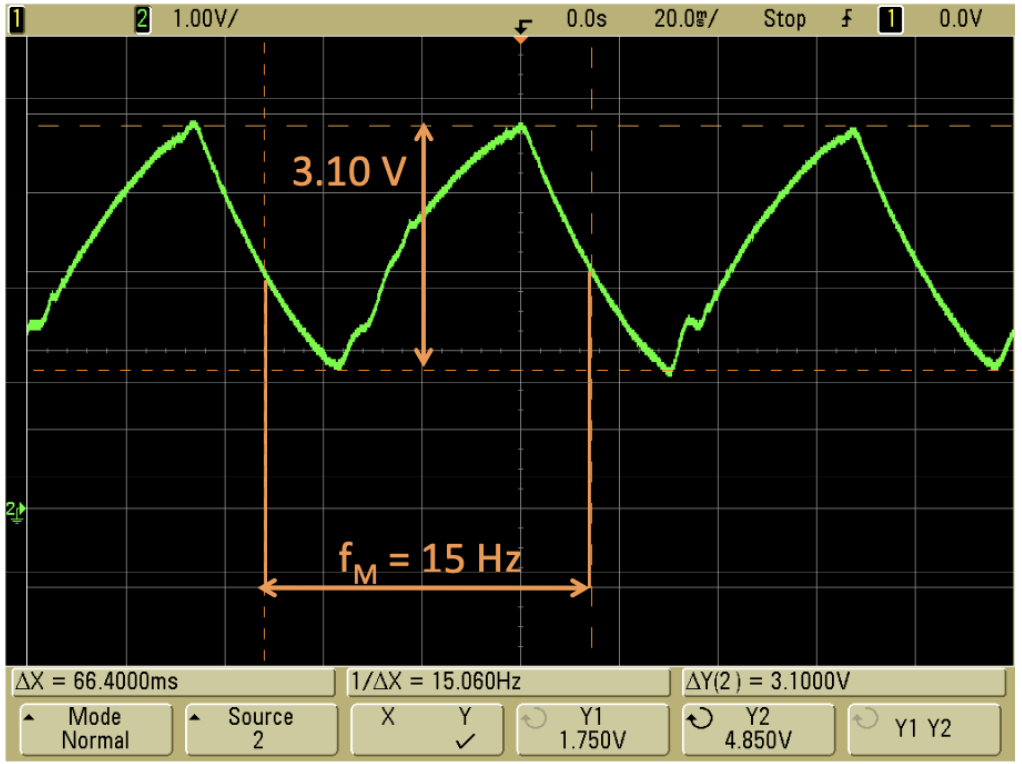
- **Carrier waveform**:
  - Square or sine wave
  - Frequency value $f_C = \frac{f_{high} + f_{low}}{2}$

- **Modulating waveform:**
  - Modulation type FM
  - Shape triangular
  - Modulation amplitude $\Delta f = \frac{f_{high} - f_{low}}{2}$
  - Modulation frequency f_m set to 1/10 of the loop 10 filter bandwidth (f_m =1 Hz)

Loop filter bandwidth effect



(a) FM with 1-Hz sinusoidal modulation



(b) FM with 15-Hz sinusoidal modulation

PLL lock and capture ranges

Phase comparator 2

- Phase Comparator I. Ensure that the jumper is placed in the right (Phase comparator II) position
- Fast loop filter

- **Free-running frequency**
  - Loop Filter BNC output close to 0

- Starting from f_{min}, the PLL will be able to lock to any frequency, up to an upper limit close to f_{MAX}

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