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Mixed-signal oscilloscope (MSO)

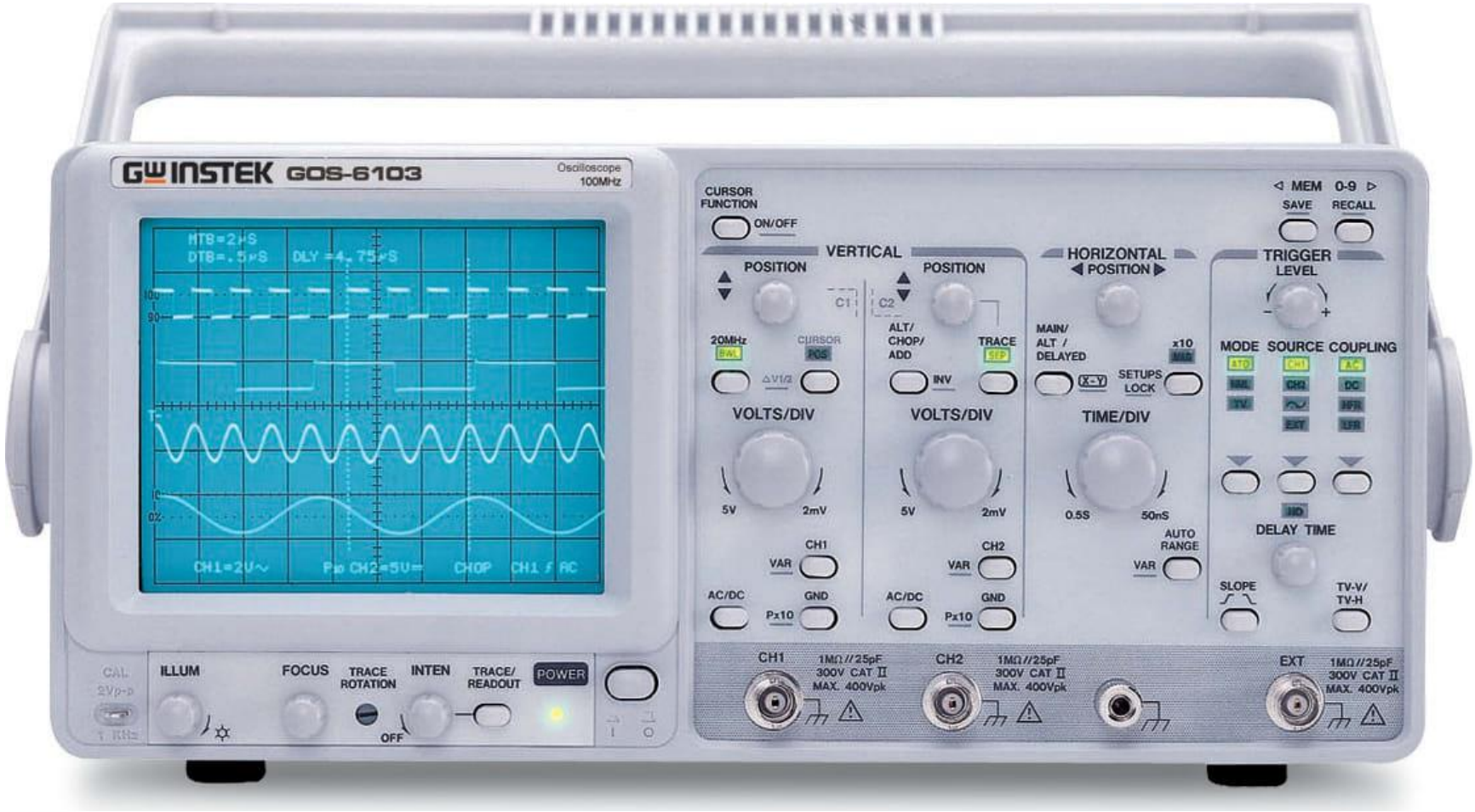
Lecture #10
Electronic measurements
Alessandro Pozzebon

Analog and digital signals

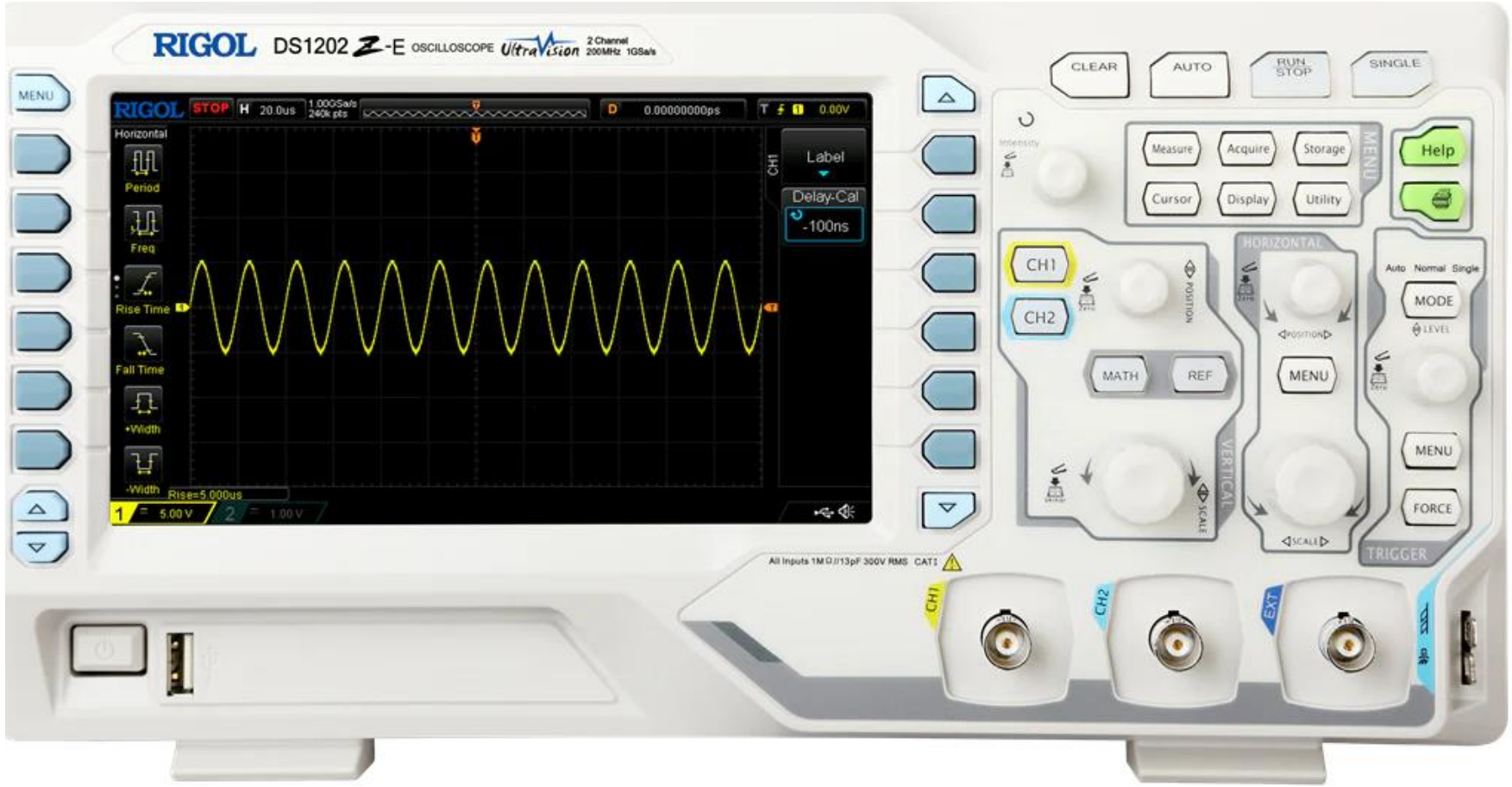
- **Analog electronics:**
  - **Complex** signals
  - Limited number

- **Digital electronics**:
  - **Simple** signals ⇒ Transitions between two levels
  - **Large** number
  - Correct **logic** combinations
  - Specified **timing** conditions

Analog electronics



Analog electronics



Digital electronics

- Digital data: sequence of **two-level voltage values**
- **Rectangular pulses**:
  - Length T_P
  - Amplitude 0 and V_P or $-V_P$ and V_P
- Clock period T_{ck}

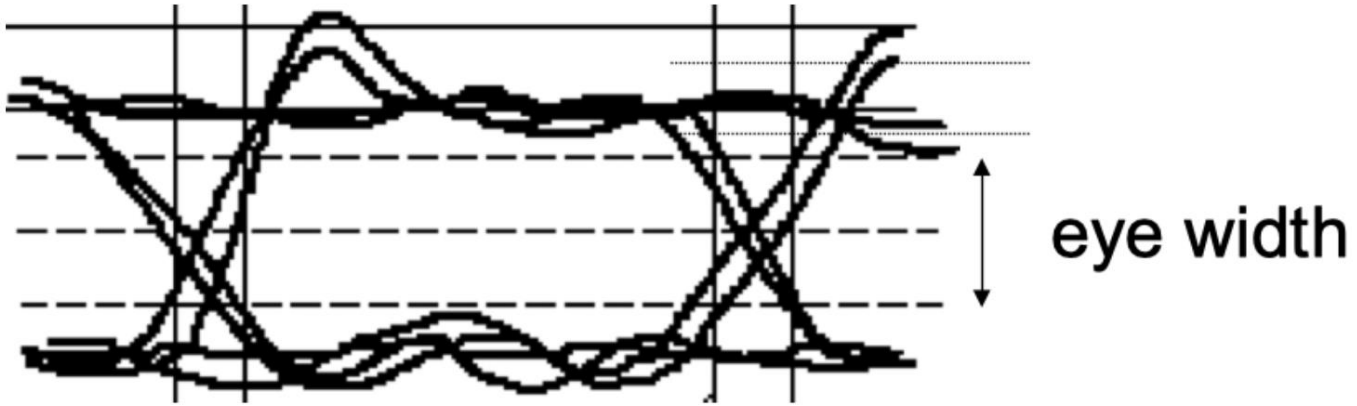
$T_P > T_{ck}$

- **Eye diagram measurement**
- Digital analysis with any **common oscilloscope**

- **Superimposition** of all the waveforms on a signal line in any interval (or in T_{ck})

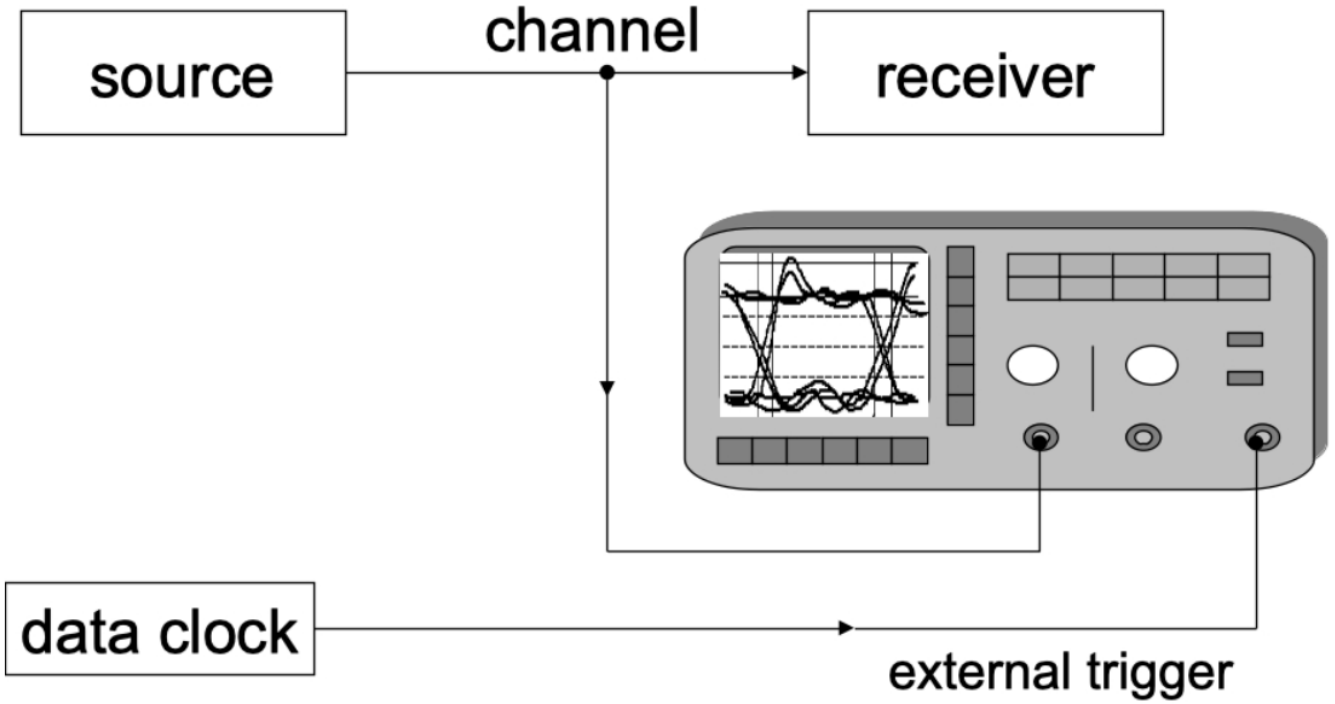
Eye diagram analysis

- Factors causing variability:
  - Switching transients caused by parasitic reactances in the circuit
  - Transients caused by **multiple signal reflections** in a high-speed logic circuit
  - **Switch time and/or propagation time variability** in digital circuits, that may depend on specific logic patterns
  - **Coupling among nearby lines** causing cross-talk



Eye diagram analysis

- **Oscilloscope settings**:
  - External trigger ⇒ data clock
  - Horizontal scale factor ⇒ little longer than the data clock period
  - Infinite persistence display



Eye diagram analysis

- Measurements and data analysis:
  - Memory ⇒ **two-dimensional trace histogram**

- Statistical process ⇒ **large number of traces**

  - **Amplitude histograms** at a given time instant

  - **Eye width**
  - **Mean voltages** at logic high and low
  - **Logic threshold** (average of the two voltages)

Eye diagram analysis

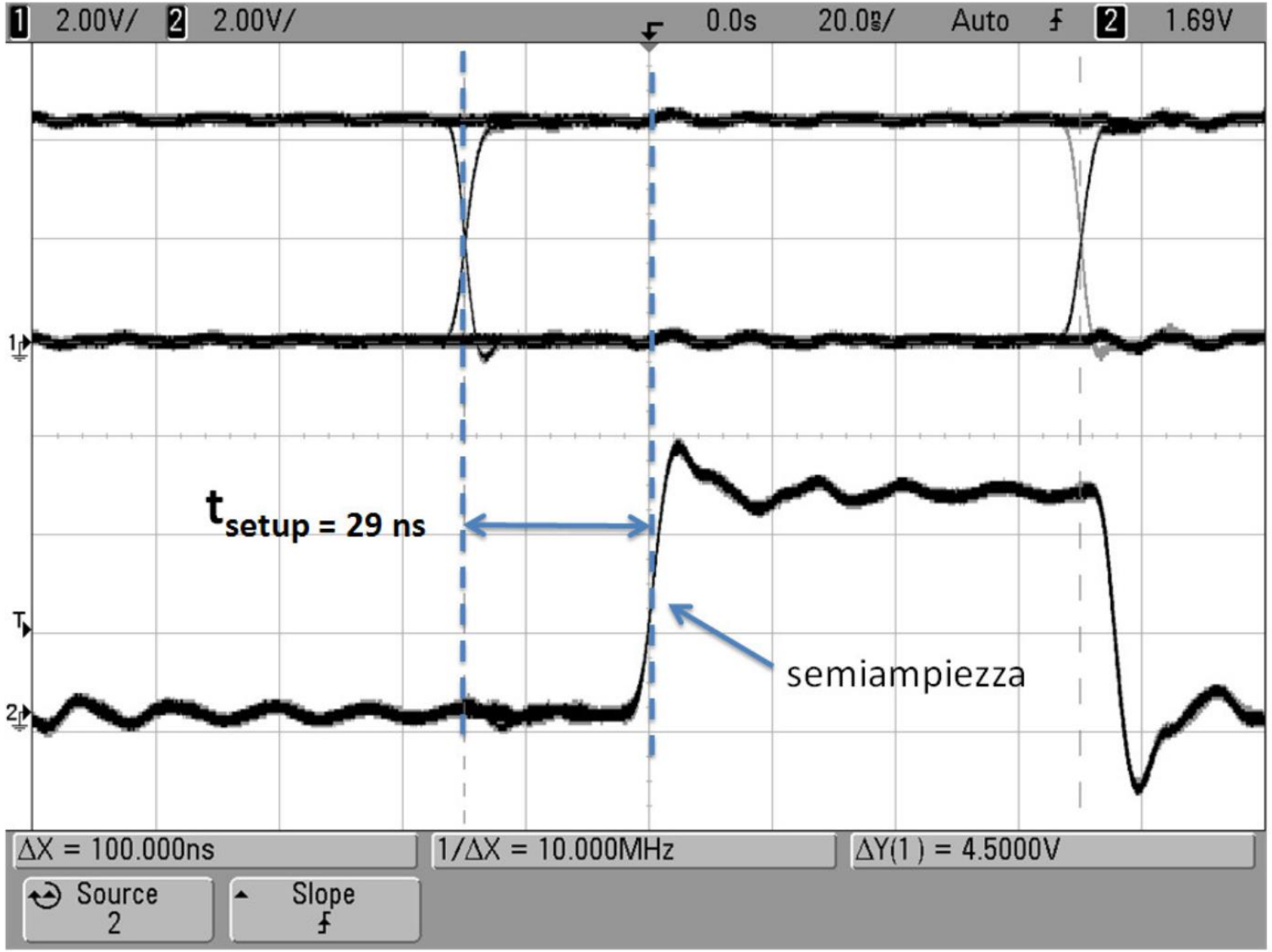
- Measurements and data analysis:
  - Memory ⇒ **two-dimensional trace histogram**

- Statistical process ⇒ **large number of traces**

  - **Time histograms** at a given amplitude level

  - **Crossing times**
  - **Data jitter**

Eye diagram analysis



Digital electronics

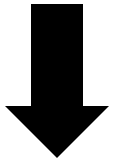
Logic analysers

- Acquisition tools for **digital signals**
- Up to **hundreds of channels**
- Compact probes (**pods**)
- Complex **triggering**
- Detection of **protocols**
- **Waveform or listing** visualization

Digital electronics

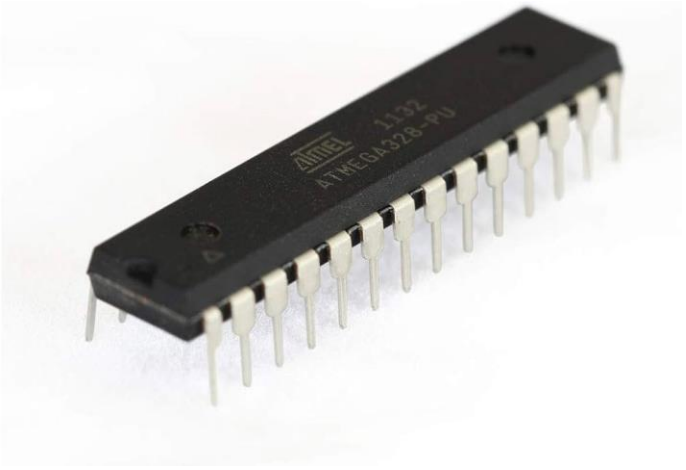
Embedded systems

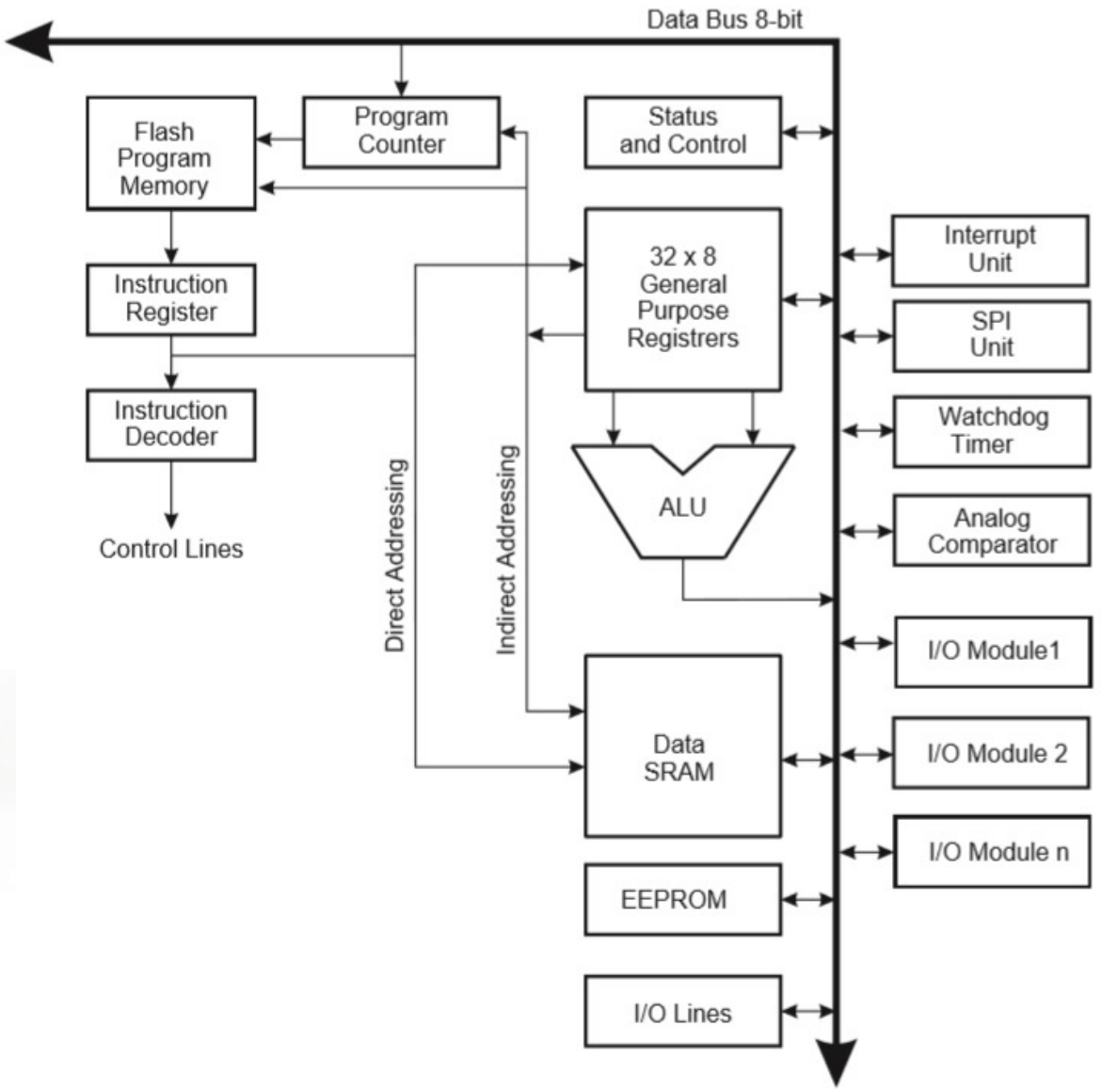
- **Dedicated systems**, designed and optimized for a specific function
- Embedded systems interact with the environment through **analog and digital interfaces**
- In embedded systems, **electrical, electronic and mechanical aspects** are strictly interrelated

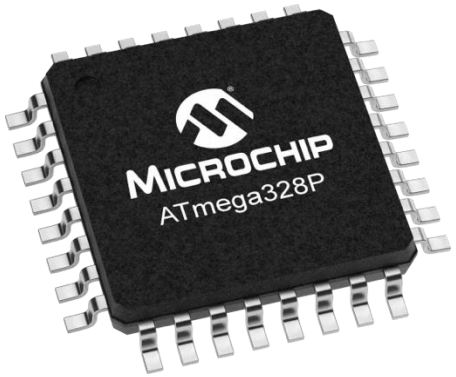


Microcontroller Units (MCUs)

Microcontrollers





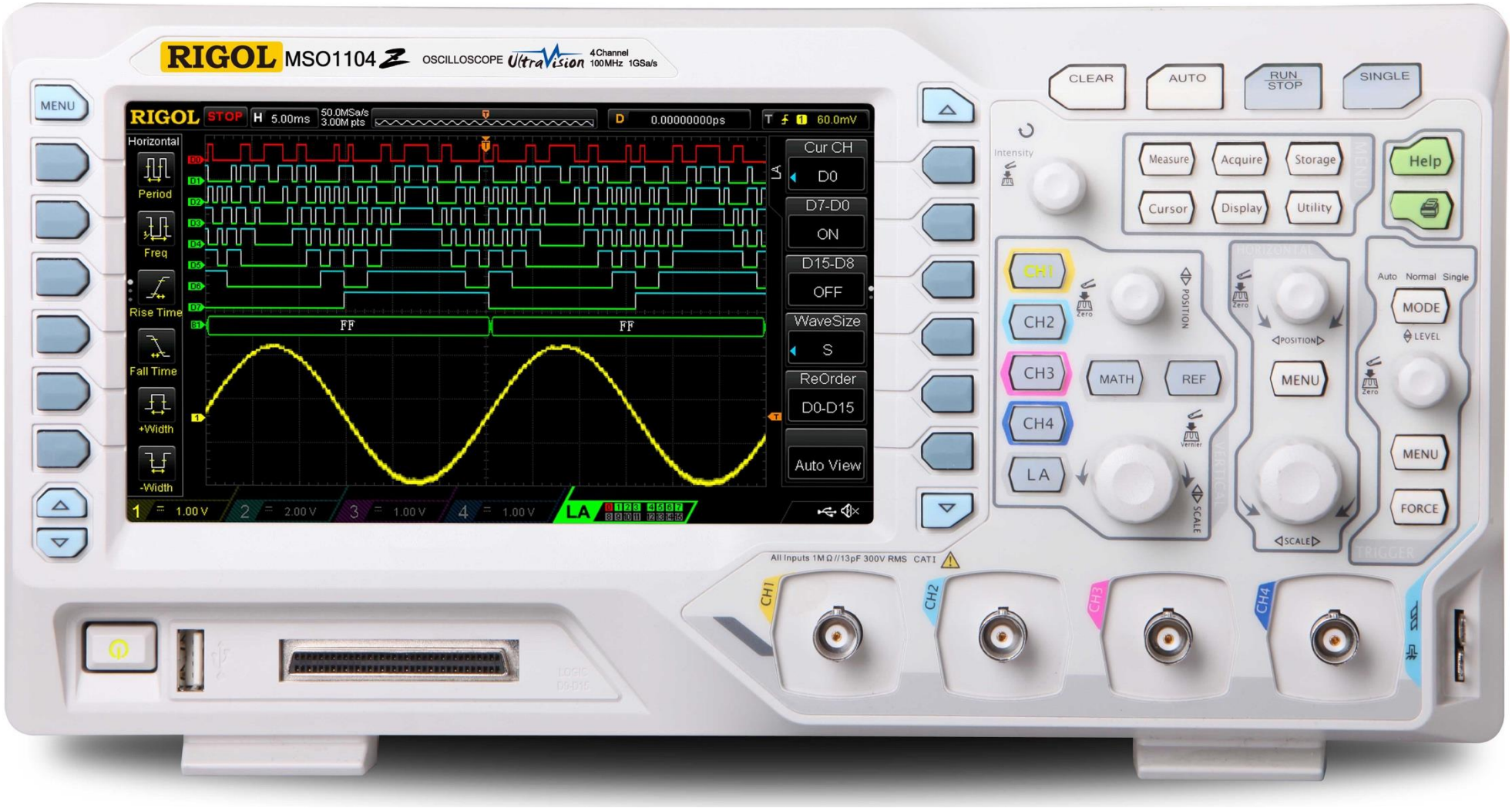


Mixed-signal oscilloscopes

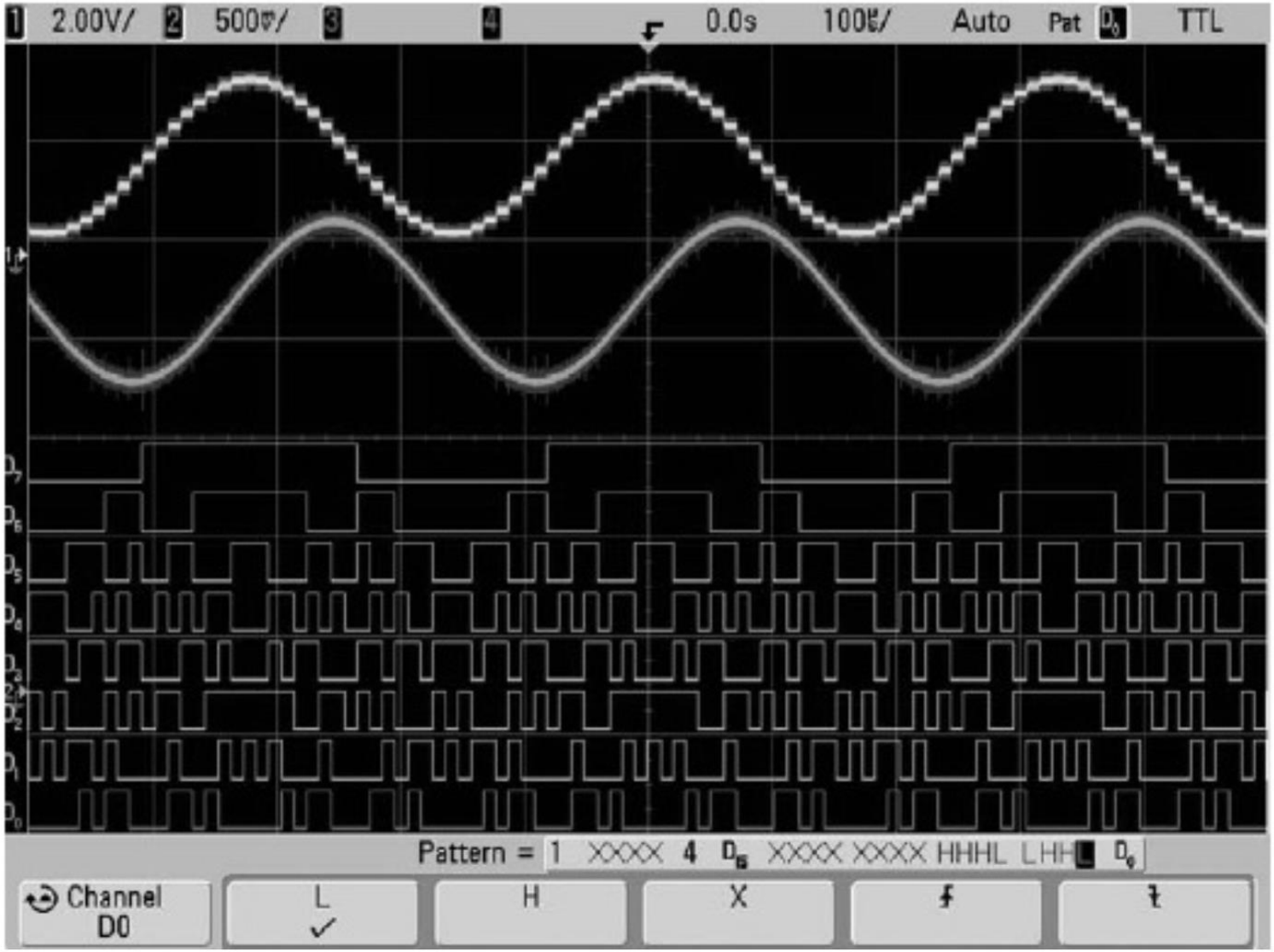
- Simultaneous acquisition of **analog and digital** signal
- Analysis of their **interrelations**
- **Hybrid** between a DSO and a logic analyser:
  - Analog inputs (2 or 4)
  - Digital inputs (typically 16) ⇒ notably lower than a logic analyzer
- **Common time reference**
- **Combined trigger** conditions

- More complex systems ⇒ **Integration of DSOs and logic analysers**

Mixed-signal oscilloscopes



Mixed-signal oscilloscopes



Digital acquisition section

- **Signals of interest**:
  - Control lines, digital I/O
  - Serial communication lines
  - Analog input and output lines
- **Basic requirements**:
  - Acquisition of signal from a number of lines
  - Compatibility with voltage and current specifications
  - Digital acquisition memory size
  - Allowance for definition of trigger conditions

Pods

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MSO Pods

- Signal conditioning
- 8 lines per pod
- High input impedance
- Variable threshold voltage comparator

- Outputs can be already considered logic-level information

Digital acquisition probes

Acquisition

- Digital inputs are acquired and stored as binary values representing two **logic states**, or «levels» (0 and 1)
- Comparator **threshold**
- **Two thresholds** (low-level and high-level) ⇒ third intermediate level
- Representation of signal transition ⇒ identify **hardware criticalities**
  - Contentions when accessing a three-state bus
  - Slow transitions
  - Metastability
  - Noise effects
- Noise margin tests ⇒ adjusting the two thresholds
- High-speed sampling clock

Time reference

- Digital systems ⇒ Synchronous logic circuits
- Timing ⇒ **System clock** ⇒ Any logic transition after a clock event
- **Clock taken from the system under test** ⇒ Only logic states and their succession can be observed
- **Anything between two clock events is ignored** ⇒ no test on correct operation of the digital hardware

- Timing analysis: verification of time relationships and device coordination

- In an MSO the acquisition clock is provided by the **instrument time base** and is shared by the analogue and digital acquisition systems
  - Comparisons between digital and analog traces on the same display

Time reference

- MSO clock rate should be at **least 5 to 10 times higher** than the clock rate in the system under test

- **Time skew**
  - small propagation time differences among channels
  - negligible unless the acquisition clock has comparable period (sampling rates in the order of GHz)

- **Inter-channel skew** among digital input lines ⇒ kept suitably low by design
- **Skew between the analogue and digital sections** ⇒ more significant (in the order of nanoseconds)
    - programmable delay lines ⇒ time alignment in the order of 100 ps

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MSO trigger

Coordinated analog and digital signal analysis

Analog and digital inputs in coordination

- **Trigger conditions as patterns** ⇒ Combination of logic values
- 4 analog and 16 digital inputs ⇒ combination of up to 20 conditions
  - Analog: specific values
  - Digital: 0, L or 1, H (or X if unassigned)

- **Pattern trigger** ⇒ logical AND operation
- Entering the pattern vs leaving the pattern

MSO trigger

- **Transient patterns (Races)** ⇒ Quick sequence of states
  - Unstable triggering

- **Time qualified pattern triggering**
  - Minimum time length: avoid transient patterns
  - Maximum time length: detect transient states or glitches

- **Protocol triggers** ⇒ protocol states
- I2C, SPI, USB…

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