# **AURIX Analog-to-Digital Converters**



restricted



Introduction to ADC

# ADC Theory

- Sampling
- Resolution
- Nonlinearities
- Dynamic range
- SAR ADC example

# AURIX ADC

- AURIX ADC Modules
- EVADC Groups & Channels
- EVADC Conversion Queue
- EVADC Initialisation Sequence



Hands-on session



ADC is a circuit that converts an analog signal (voltage variation over time) into discrete form (digital values) that can be processed by HW or SW





### **Conversion pipeline**



### **Key Characteristics**

- Sampling Rate
- Resolution
- DC & AC nonlinearities
- Dynamic range
- Supply level, consumption
- Input types
- Output format



# The **sample rate** or sampling frequency is the maximum rate at which an ADC can convert the analog signal into a digital data



ADC sample conversion time ( $T_{CONV}$ ) = Sampling time ( $T_{SMPL}$ ) + Bit conversion time ( $T_{SAR}$ )

ADC sample rate =  $1/T_{CONV} = 1/(T_{SMPL} + T_{SAR})$ 

The sampling interval is a part of the sampling-conversion period at which an ADC <u>stores and holds</u> (SH) an instantaneous value of the input signal



The selection of the Sampling rate depends on the input signal's highest frequency component (fa) and is defined by the **Nyquist frequency** (fs):

### *f*s≥*f*a\*2

Understanding the input signals properties e.g. highest frequency content is an important part of getting accurate measurements and avoiding Aliasing





# The resolution determines the minimum change in the input signal that makes the output change by one count

The resolution is expressed as a number of output bits. The smallest increment in the signal value that can be recognized by an ADC is defined as *least significant bit* (LSB):

Resolution, N	2 <sup>N</sup>	LSB
8bit	255	10 mV
10bit	1024	5 mV
12bit	4096	1.22 mV
14bit	16384	0.3 mV
16bit	65536	0.075 mV



Vref = 5V



# Transfer function nonlinearities in a real ADC



Total Unadjusted Error (TUE) defines the maximum deviation (in LSBs) from the ideal transfer curve

 $TUE = \sqrt{Offset^2 + Gain^2 + DNL^2 + INL^2}$ 



Dynamic range defines the ratio between the minimum and the maximum input values that an ADC can reliably convert



SAR ADC



This sampled input from Sample & Hold (SH) capacitor is fed into a comparator along with the input from an internal DAC, the output of which is adjusted in binary increments to get as close as possible to the sampled value



SAR ADC employs a binary search algorithm to match an input voltage with a reference value



#### 4-bit conversion example



### Three ADC types in AURIX

- SAR x 12 by 8/16 channels
  - **EVADC** Primary 12 bit,  $\leq 2.5$ MS/s
  - **EVADC** Secondary 12 bit,  $\leq$  1.4MS/s
- <u>Fast Compare</u> x8 10 bit, ≤ 5MS/s
- <u>EDSADC</u> x14 16 bit, ≤ 200KS/s

## TC375: 8 x EVADC, 4 x FCC, 6 x EDSADC







Each **EVADC Group** is an independent SAR converter that consists of 8 (or 16) input channels, Multiplexer, Converter, Control Logic, Request control and Result handling

EVADC input channels are multiplexed to connect the corresponding signal source to the converter one at a time. For each channel, the sample time can be controlled individually







# EVADC Conversion

# EVADC is designed to execute complex sequences of conversions by filling up <u>Queues</u>

#### **Conversion Request**

Conversion sequence can be started (requested) by 3 different sources:

- Software Trigger
- Self-Timed Trigger,
- External Trigger e.g. GPIO, GTM

The requested conversion can be executed once or repeatedly after trigger

#### <u>Arbiter</u>

When multiple conversion requests are used arbitration process defines which conversion is executed next based on assigned priorities





#### Enable a primary/secondary group and prepare it for operation **EVADC** basic setup sequence EVADC GxANCFG = $0 \times 00300000$ ;Analog clock frequency is 160 MHz / 4 = 40 MHz (example) ; CALSTC = 00EVADC GxARBCFG = 0x0000003 ;Enable analog block Clk & Analog Block enable WAIT ; Pause for extended wakeup time ( $\geq$ 5 µs) ;Begin start-up calibration EVADC GLOBCFG = $0 \times 8000000$ ; (other operations can be executed in the meantime) :Enable arbitration slot 0 EVADC GxARBPR = 0x0100000 Request source and queue settings EVADC GxQMR0 = 0x0000001 ;Enable request source 0 EVADC GxICLASS0=0x0000002 ;Select 4 clocks for sampletime 4 / 40 MHz = 100 ns Sample time settings ;The default setting stores results in GxRESO, ;service requests are issued on GxSR0 ;Enable result service requests, if required EVADC GxRCR0 = 0x8000000;Request channel 0 in auto-repeat mode EVADC GxQINR0 = 0x00000020 ;Wait for start-up calibration to complete WAIT ; (other operations can be executed in the meantime) Start conversion ;---> This starts continuous conversion of the channel

Wait for the 1<sup>st</sup> conversion result



# ADC\_Single\_Channel\_1 for KIT\_AURIX\_TC375\_LK





## <u>Books</u>

Walt Kester. 2003. Mixed Signal and DSP Design Techniques, Analog Devices, ISBN 978-0-7506-7611-3

Thomas C. Hayes. 2016. Learning the Art of Electronics: A Hands-On Lab Course 1st Edition, Cambridge U. Press, ISBN 978-0-521-17723-8

## **Application Notes**

AP56003 A Guide to the Analog Part of the A/D Converter

AP32297 A/D Converter Supply and PCB Design Guideline

# **Code examples & Tutorials**

https://github.com/Infineon/AURIX\_code\_examples/blob/master/code\_examples

https://www.infineon.com/cms/en/product/promopages/aurix-expert-training/



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