Evaluation Board

For AURIX™ Family

AURIX™ lite Kit V2

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Board User's Manual

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 2020, October	Initial released Version is V2.0
Revision 2021, September	Corrected Version V2.1
Page 13	Add SO8-150 as specific package
Page 18, Figure 7	Order on X301 corrected (mirrored)
Page 26, Figure 14	Add footnote about wrong printing of P11.6
Revision 2022, April	Corrected Version V2.2
Page 12	Add description of CAN_STB

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1 Introduction

This document describes the features and hardware details of the **AURIX™ lite Kit V2** equipped with a **32-Bit Single-Chip AURIX™ TriCore™-based Microcontroller TC375, TC365, TC275 or TC265** from Infineon Technologies AG.

It can be used with a range of development tools including Infineon's free of charge Eclipse based IDE **AURIX™ Development Studio** or the Eclipse based **"FreeEntryToolchain"** from HighTec/PLS/Infineon**.** AURIX™ Development Studio is a comprehensive environment, including C-Compiler and Multi-core Debugger, Infineon's low-level driver (iLLD), with no time and code-size limitations that enables editing, compiling and debugging application code. The FreeEntryToolchain is a full C/C++ development environment which has a source-level UDE debugger from PLS included and is also based on Infineon low-level driver (iLLD).

Table 1 shows the overview specifications of the whole board.

Table 1 Overview of the Board Specification

CPU Core AURIX™	Manufacturer Order No.	SAK-TC375TP-96F300W AA
	Manufacturer Order No.	SAK-TC365DP-64F300W AA
	Manufacturer Order No.	SAK-TC275TP-64F200W DC
	Manufacturer Order No.	SAK-TC265D-40F200W BC
Board Dimensions	66.0 x 131.0 mm	
Power	• on-board miniWiggler Micro-AB USB interface • external powering 5 V…40 V (recommended 7 V...14 V)	
Connectors	• Most AURIX™ pins available on expansion connectors (X1, X2) • Two Infineon Shield2Go connectors • Arduino compatible connectors for 3.3 V • mikroBUS™ connector • Micro-USB connector • DAP Debug connector • CAN connector • RJ45 connector	
Others	• CAN transceiver TLE9251VSJ from Infineon • Low Power 10/100 Mbps Ethernet Physical Layer Transceiver DP83825I from TI • 1 user push-button, 3 user LEDs • Reset push-button • Potentiometer (10 kOhm) for variable analog input	

These boards are neither cost nor size optimized and do not serve as a reference design.

1.1 Block Diagram

- The block diagram in Figure 1 shows the main components of the AURIX™ lite Kit V2 and their interconnections.

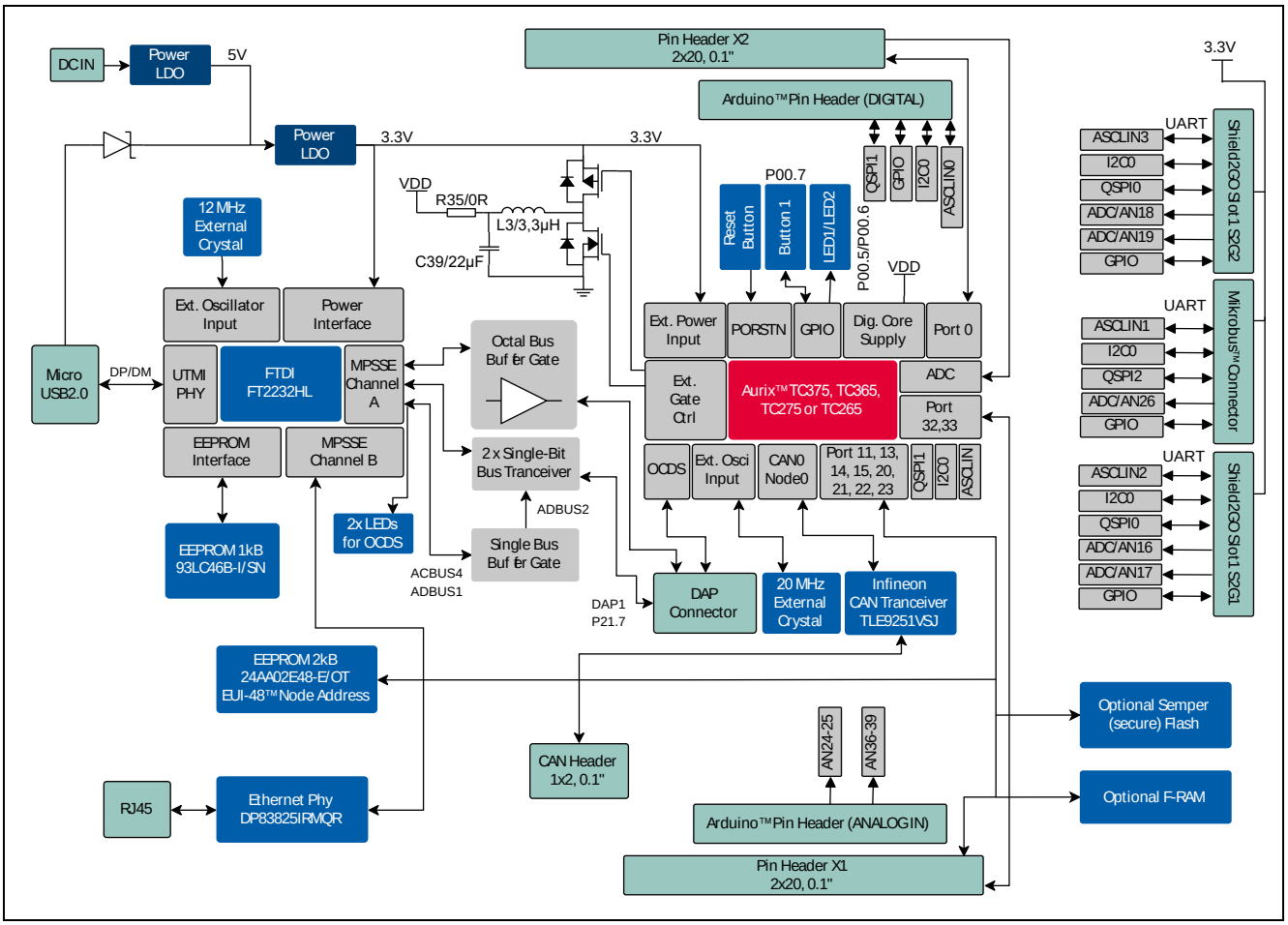


Figure 1 Block Diagram of the AURIX™ lite Kit V2

2 Hardware Description

The following chapters give a detailed description of the board hardware and how it can be used. The different parts of the kits series are shown in Figure 2 and 3.

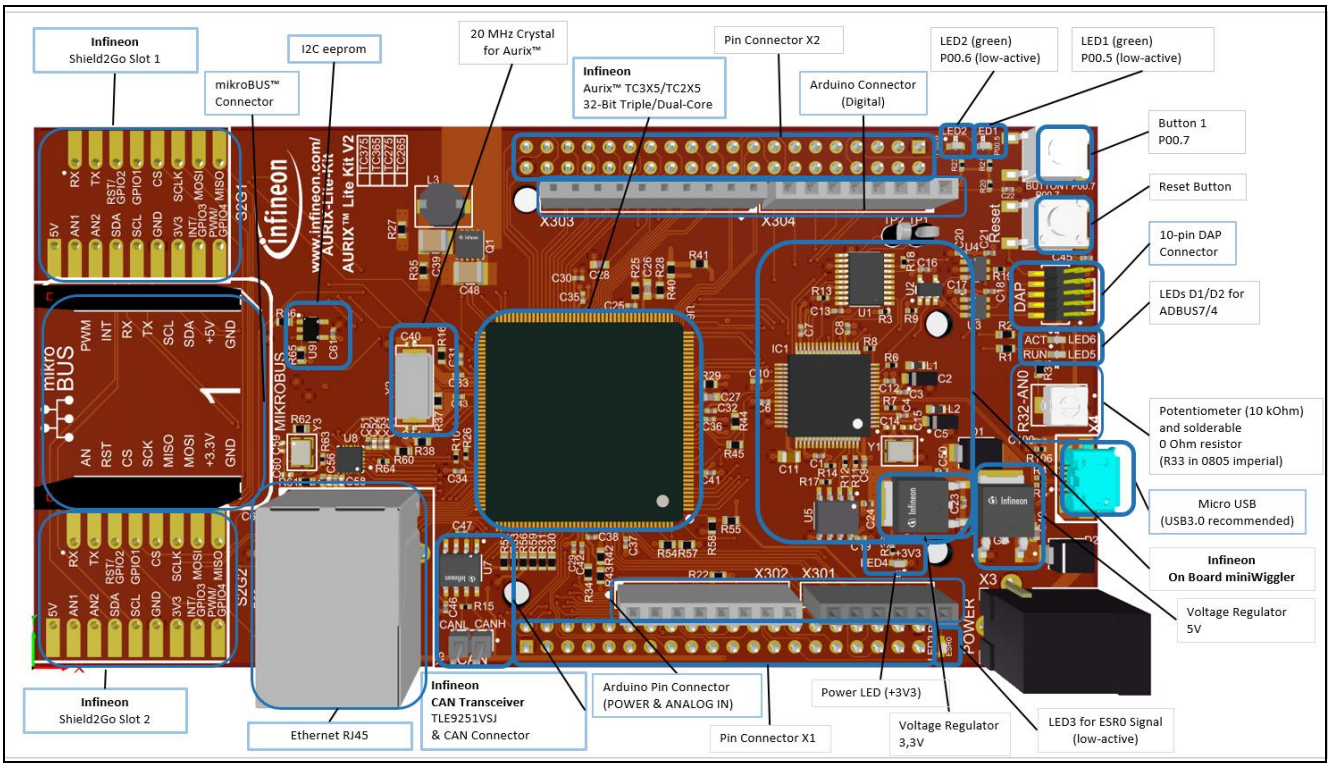


Figure 2 AURIX™ lite Kit Board V2 View from the Top

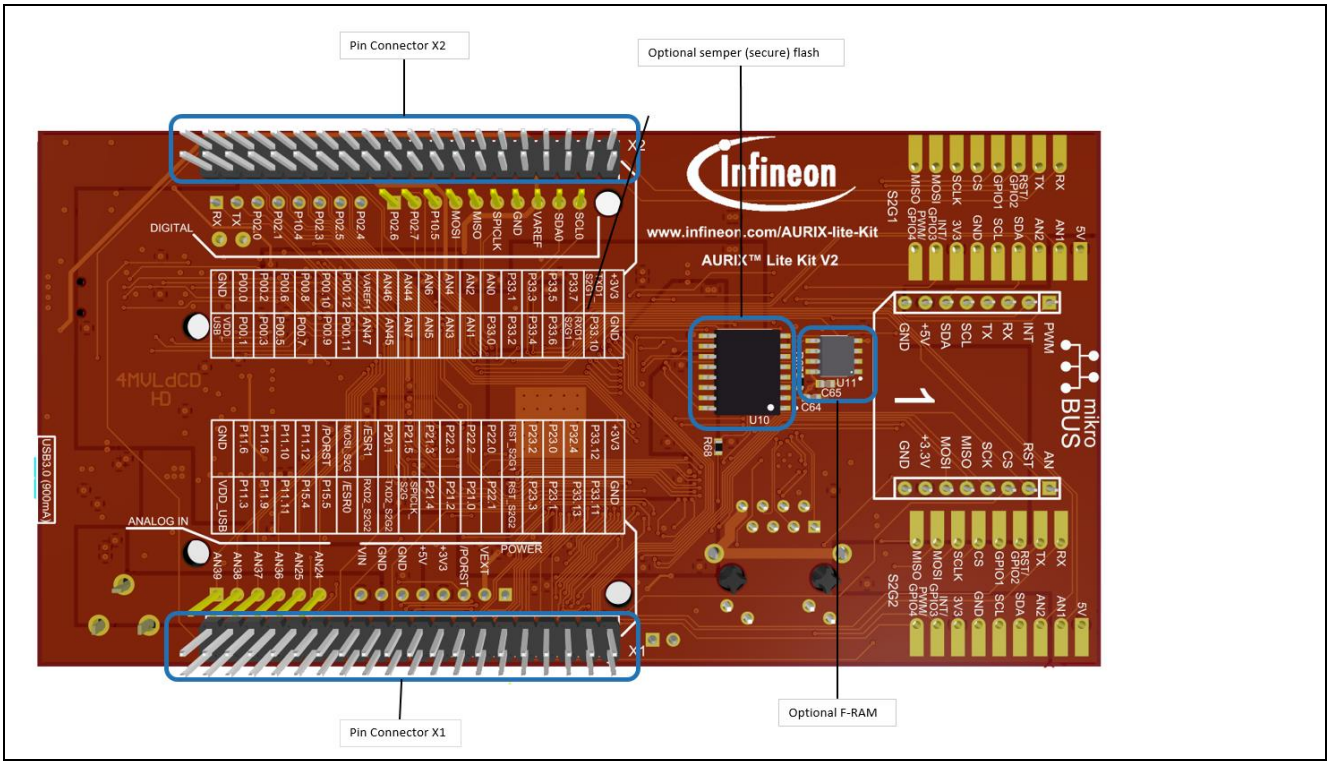


Figure 3 AURIX™ lite Kit Board V2 View from the Bottom

2.1 Power Supply

The AURIX™ lite Kit V2 must be supplied by an external DC power supply, this can be done via the DC plug X3 (recommended voltage range +7 V…+14 V) or via the micro USB plug X4 (+5 V).

The green Power LED4 indicates the presence of the generated 3.3 V supply voltage.

For X3 you can use a female DC supply plug with outside diameter of 5.5 mm and inside diameter of 2.1 mm or 2.5 mm. The inner contact is positive and the outer contact is ground.

In case that the board is powered via the micro USB plug X4, the used voltage will be always less than 5 V (~4.5 V) because the USB voltage is protected by a schottky diode (D1). Therefore also it is possible to use X3 and X4 on the same time. As long the voltage on X3 is higher than +7 V the board is powered via X3. If the voltage on X3 is less than +5.5 V the board is powered via X4. Between +5.5 V and +7 V on X3 the board is powered from X3 and X4 together.

If the board is powered via a USB plug and/or the DC plug, it's not recommended to apply an additional power supply to one of the power pins (VEXT, +5V, +3V3, VDD_USB) on the pin headers X1, X2, the Arduino Power header X302, the Shield2GO slots or the mikroBus™ connectors, because there is no protection against reverse current into the external power supply. These power pins can furthermore be used, to power an external circuit and therefore used as an output. But care must be taken to not draw more current than USB can deliver. A PC as USB2.0 host typically can deliver up to 500 mA current and USB3.0 up to 900 mA. For best performance, we recommend to use USB3.0. If higher currents are required and in order to avoid damages on the USB host, the use of an external USB power supply unit, which is able to deliver higher currents, is possible.

Note: *The LDO G1, that transfers the 5 V to 3.3 V, and LDO G2, that transfers VIN to 5 V, has a maximum output current rating of 1 A. Therefore, the maximum current consumption is limited to 1 A. Do not apply any additional voltage on the supply pins, because they are directly connected to the output of the LDO G1/G2 and further backwards voltage can damage or destroy the LDO. Furthermore, do not apply multiple sources on the power pins, otherwise you risk to damage and destroy the board.*

However, more options are possible, but therefore, caution is necessary, to avoid any damage to the board and your supplies. Please ensure that X4 is **not** supplied by any power source or PC, for all mentioned configurations below. Otherwise, **you risk to damage your source or PC**.

Ensuring the mentioned points, following supply options are possible with a +5 V power source:

- Option 1: Supply +5 V on the +5V pin at X302 Arduino power connector
- Option 2: Supply +5 V on either one of the VDD_USB pins at X1 or X2 connector
- Option 3: Supply +7 V…+14 V on the VIN pin at X302 Arduino power connector

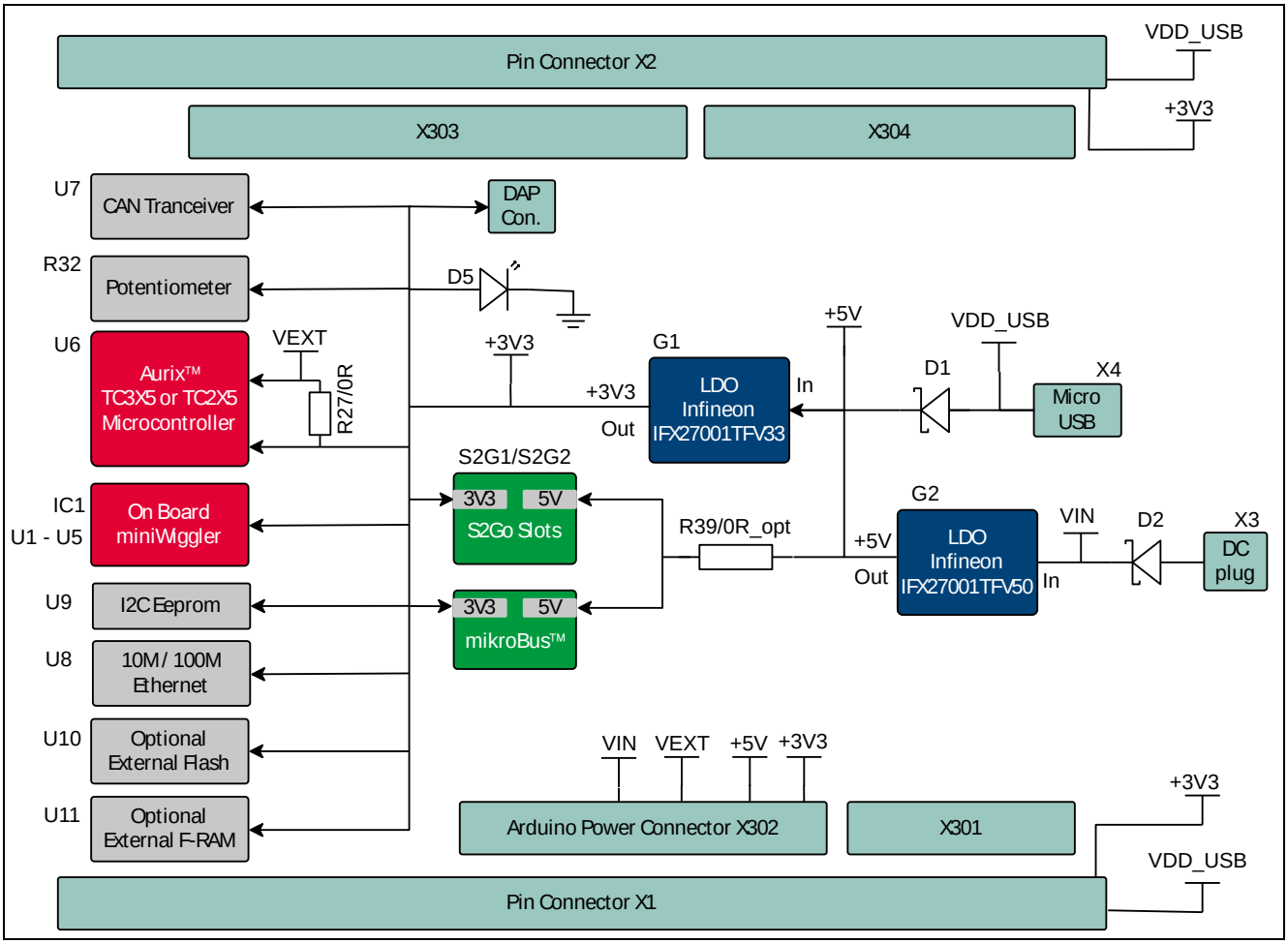


Figure 4 Power Supply Concept

Note: *Do **not** apply any voltage on the mentioned power pins, if the USB is plugged in or any voltage is applied via DC plug. Furthermore, do not apply multiple sources on the power pins, otherwise you risk to damage and destroy the board.*

2.2 User Push Buttons, User LEDs and Potentiometer

The **AURIX™ lite Kit V2** provides one user push button, a reset button, two LEDs and one potentiometer. Additionally, LED3 can be used for visualizing an emergency stop function at ESR0 (emergency service request). The LEDs LED5 and LED6 are used for visualizing activites via the on-board miniWiggler. The port pins used can be found in Table 2 and Table 4.

Table 2 AURIX™ Pin Mapping for User LEDs

Name	AURIX™ Pin	Color	Active
LED1	P00.5	green	Low-active (pull against GND)
LED2	P00.6	green	Low-active (pull against GND)
LED3	ESR0	red	Low-active (pull against GND)

Table 3 miniWiggler Pin Mapping for User LEDs

Name	miniWiggler Pin	Color	Active
LED5	ADBUS4 (ACTIV)	green	Low-active (pull against GND)
LED6	ADBUS7 (RUN)	green	Low-active (pull against GND)

Table 4 AURIX™ Push Buttons and Potentiometer

Name	AURIX™ Pin	Active
Button1	P00.7	Low-active (pull against GND)
Reset	/PORST	Low-active (pull against GND)
R32 (10kΩ)*	AN0	-

*Note: Desoldering resistor R33, enables AN0 for other functions, but disables the Potentiometer functionality.

2.3 Debugging and on board miniWiggler

The **AURIX™ lite Kit V2** supports debugging via 2 different channels:

- On-board miniWiggler via the the microUSB X4
- 10-pin DAP Connector

2.3.1 USB Connector

The USB connector is used for connection to a PC. Via the USB it is possible to power the board, using the ASCLIN0 as serial connection via USB and Debugging via DAS.

NOTE: Before connecting the board to the PC, make sure that the actual DAS software is installed on the PC.

For actual DAS software please contact your local FAE.
The software can also be found on:

DAS website

2.3.2 Serial Connection to PC

After the first connection of USB to a PC the needed driver will be installed automatically. During this there will be created a new COM port on PC. This COM port can be used to communicate with the board via ASCLIN0 of the device and ASCLIN4 (TC3X5 only) if R44 and R45 are assembled. Per default the ASCLIN0 is used on P14.0 and P14.1 (e.g. Generic Bootstrap Loader). Because ASCLIN0 is used also for the Arduino pins, you can use here also ASCLIN4 to use it in parallel, make sure that P14.0/P14.1 are not configured in this case.

2.3.3 miniWiggler JDS

The miniWiggler JDS is a low cost debug interface which allows you access to the device via DAP. Make sure that you have the latest DAS release. Debugging is possible via the DAS Server 'UDAS'. Please contact your preferred debug vendor for support of DAS. If you have connected the board to the PC and there runs the DAS server, then a working connection is visible via the green LED5 (ADBUS4). The status LED6 (ADBUS7/green) is switched on/off through the DAS Server, depending on the used debugger (client).

IMPORTANT: Make sure that there is no or a tristated connection on the DAP connector if the LED5 (miniWiggler in use) is on.

2.4 Reset

The power on reset input pin (/PORST) of the AURIX™ family is a bi-directional input/output intended for external triggering of power-related resets. If the PORST pin remains asserted after a power event then the reset will be extended until it is deasserted. This does not replace the ESR pins functional reset. An internal pull-up resistor (2.2 kΩ) keeps the PORST# pin high during normal operation. A low level at this pin will force a hardware reset. In case of a MCU internal reset the PORST# pin will drive a low signal.

A reset signal can be issued by

- the on-board Reset Button ("RESET")
- the on-board miniWiggler via IC FT2232HL (IC1.27 – ACBUS1)
- the on-board DAP connector (DAP.10)
- the Arduino Power Header (X302.3, "/PORST")
- the pin header X1 (X1.30, "/PORST")

An AURIX™ internal circuit always ensures a save Power-on-Reset. AURIX™ lite Kit V2 does not require any additional external components to generate a reset signal during power-up. For more informations, please refer to the datasheet or user manual of the assembled AURIX™ device.

2.5 CAN Transceiver

The **AURIX™ lite Kit V2** provides a CAN interface via the CAN connector. The TLE9251V is the latest Infineon high-speed CAN transceiver generation, used inside HS CAN networks for automotive and also for industrial applications. It is designed to fulfill the requirements of ISO 11898-2 (2016) physical layer specification and respectively also the SAE standards J1939 and J2284. The CAN buses (signals CANH, CANL) are terminated with by a 120 Ohm resistor. The transceiver is connected to the TriCore™ device CAN node 0. The transceiver is in stand-by mode per default. To switch the transceiver to normal operating mode the pin CAN_STB must be driven low from the CPU. To use the CAN pins see Table 5.

Table 5 CAN Signals and AURIX™ Pin Mapping

Signal Name	Pin No. at CAN Pin Header	AURIX ™Pin, AURIX™ Function	Ass. Reg./ I/O Line
CANH	1	-	-
CANL	2	-	-
CAN_TX	-	P20.8, CAN node 0 output	TXDCAN0
CAN_RX	-	P20.7, CAN node 0 input	RXDCAN0B
CAN_STB	-	P20.6, GPIO	P20.6 OUT

2.6 I2C Eeprom

The **AURIX™ lite Kit V2** provide a 2 Kb I2C Serial EEPROM with Pre-Programmed EUI-48™ MAC ID (Microchip 24AA02E48). The slave address of this EEPROM is fixed 0x50. The upper half of the array (80h-FFh) is permanently write-protected. Write operations to this address range are inhibited. Read operations are

not affected. This upper half contains the preprogrammed EUI-48™ node address which can be used as MAC ID for Ethernet. The other 128 bytes are writable and usable by the user.

2.7 Ethernet

The **AURIX™ lite Kit V2** provide a RJ45 connector (X5) for twisted pair ethernet connections.The board use a DP83825I Low Power 10/100 Mbps Ethernet Physical Layer Transceiver from Texas Instruments as physical interface device. For more information about the ethernet modul see AURIX™ User's Manual, about the PHY see the DP83825I datasheet from TI website.
For the connection between AURIX™ and PHY is used RMII.
For the MD connection (e.g. for PHY configuration) there is used P21.2 and P21.3.

2.8 Optional Cypress Semper™ (Secure) Flash

The **AURIX™ lite Kit V2** provide the possibility to assemble an external flash. Usable devices are Cypress Semper™ NOR Flash Device Family S25HL and Cypress Semper™ Secure NOR Flash Device Family S35HL in SOIC-16 package. For more information about the flashs please see https://www.cypress.com/products/semper-nor-flash-memory and https://www.cypress.com/event/semper-secure-nor-flash-memories. If you assemble a flash then assemble also the ceramic capacitor C64 with 100 nF (size 0603) and the resistor R67 with 0 Ω (size 0603). In case of use a Semper™ Secure NOR Flash you can also assemble the resistor R67 with 0 Ω (size 0603) to connect the interrupt output of the flash to the AURIX™ pin P20.9 (SCU_REQ7 on TC3X5; SCU_REQ11 on TC2X5). The AURIX™ support only single SPI protocol, Dual and Quad SPI protocol is not possible.

The flash is connected to P22.0, P22.1, P22.3 (QSPI4 on TC3X5; QSPI3 on TC2X5). Pin P22.2 (Slave Select Output 3 of QSPI4 on TC3X5; Slave Select Output 12 of QSPI3 on TC2X5) is used as slave select.

Please note that the used QSPI is shared with the optional F-RAM (see Optional F-RAM).

2.9 Optional F-RAM

The **AURIX™ lite Kit V2** provide the possibility to assemble an external serial F-RAM. Usable devices are Cypress F-RAM FM25VN10-G and Cypress F-RAM Serie CY15B in SOIC-8 package (SO8-150). For more information about the F-RAMs please see https://www.cypress.com/products/f-ram-nonvolatile-ferroelectric-ram.

If you assemble F-RAM then assemble also the ceramic capacitor C65 with 100 nF (size 0603).

The F-RAM is connected to P22.0, P22.1, P22.3 (QSPI4 on TC3X5; QSPI3 on TC2X5). Pin P23.1 (Slave Select Output 6 of QSPI4 on TC3X5; Slave Select Output 13 of QSPI3 on TC2X5) is used as slave select.

Unfortunately there is no connection on pin 3 (#WP) and pin 7 (#HOLD) of the F-RAM. Please check the datasheet if the used F-RAM has internal weak pull-up connected or need an external connection to VDD. If external connection is needed then make such a connection via wire wrap line.

Please note that the used QSPI is shared with the optional flash (see Optional Cypress Semper™ (Secure) Flash).

3 Configuration

3.1 Bootmode

Table 6 User Startup Modes [1)2)]

HWCFG[5...3]	Type of Boot	R58	R57	R59
XX1	Start-up mode is selected by Boot Mode Index	X	X	NA
110	Internal Start from Flash	NA	NA	A
100	Alternate Boot Mode, Generic Bootstrap Loader on fail (P14.0/P14.1)	A	NA	A
000	Generic Bootstrap Loader (P14.0/P14.1)	A	A	A

1) The shadowed line indicates the default setting.
2) 'A' means assembled, 'NA' means not assembled, 'x' represents the don't care state.

Please see also Table 8.

3.2 Config Signals

Table 7 Config Signals

Short Name	Description	Comment
P14.6	HWCFG0 (LDO / DCDC)	Only with TC2X5, resistor R30 (4.7 kΩ/0603 imp) pulls signal against GND (DCDC) and is assembled initially if board is using TC2X5.
P14.5	HWCFG1 (EVR33ON / EVR33OFF)	Resistor R31 (4.7 kΩ/0603 imp) pulls signal against GND (EVR33OFF) and is assembled initially.
P14.2	HWCFG2 (EVRCON / EVRCOFF)	Resistor R52 (4.7 kΩ/0603 imp) must be assembled if R59 is assembled (GPIOs are set to tri-state) and TC2X5 is used (TC3X5 has internal pull-up).
P14.3	HWCFG3 (see boot configuration Table 6)	-
P10.5	HWCFG4 (see boot configuration Table 6)	-
P10.6	HWCFG5 (see boot configuration Table 6)	-
P14.4	HWCFG6 (GPIOs pull-up / tri-state)	Resistor R59 (4.7 kΩ/0603 imp) pulls signal against GND (GPIOs in tri-state after reset) and and is not assembled initially.

3.3 Optional resistors

Some resistors/bridges enable/disable or changing functions of specific signals in Table 8.

To disable the signals, the resistors have to be removed. To enable, the resistor has to be assembled.

For example: Desoldering the intialy assembled resistor R33, disables the Potentiometer and the analog Signal AN0 of the AURIX™, making it usable for other purposes.

Table 8 Signal mapping of the optional resistors

Resistor	Res.	Assembled	Signal	Size (imperial)	Comment
R33	0 Ω	yes	AN0	0603	Disassemble to disable the potentiometer
R37	0 Ω	yes	XTAL2	0603	Serial resistor to reduce oscillator amplitude if needed.
R39	0 Ω	no	+5V	0603	Assemble to connect 5V to Mikrobus and Shield2Go connector
R59	4.7 kΩ	no	HWCFG6/P14.4	0603	Assemble to disable the internal pull-ups with power on
R52	4.7 kΩ	No	HWCFG2/P14.2	0603	Assemble to enable the EVR13, only needed with TC2X5 and R59 assembled
R53	4.7 kΩ	no	HWCFG3/P14.3	0603	Assemble to boot from BMI, only needed with TC2X5 and R59 assembled
R56	4.7 kΩ	no	HWCFG3/P14.3	0603	Assemble to select boot from HWCFG4/5, valid setting on P10.5/P10.6 needed
R54	4.7 kΩ	no	HWCFG4/P10.5	0603	Set HWCFG4 to high, only needed with R56 assembled, not with R57
R55	4.7 kΩ	no	HWCFG5/P10.6	0603	Set HWCFG5 to high, only needed with R56 assembled, not with R58
R57	4.7 kΩ	no	HWCFG4/P10.5	0603	Set HWCFG4 to low, only needed with R56 assembled, not with R54
R58	4.7 kΩ	no	HWCFG5/P10.6	0603	Set HWCFG5 to low, only needed with R56 assembled, not with R55
R44	0 Ω	no	P14.1, P00.12	0603	Assemble to use ASCLIN4 (P00.12) instead of ASCLIN0 (P14.1) via USB, only with TC3X5, P14.1 not usable in this case
R45	0 Ω	no	P14.0, P00.9	0603	Assemble to use ASCLIN4 (P00.9) instead of ASCLIN0 (P14.0) via USB, only with TC3X5, P14.0 not usable in this case

4 Connector Pin Assignment

4.1 Pinout of X1 and X2 connectors

The pin headers X1 and X2 can be used to extend the evaluation board or to perform measurements on the AURIX™ TC3X5/TC2X5. Figure 5 shows the available GPIOs / signals at these pin headers. The pin table is also printed onto the bottom side of the PCB.

Pin Header X1

	GND	1	2	+3V3	
	P33.11	3	4	P33.12	
	P33.13	5	6	P32.4[1)]	
	P23.1	7	8	P23.0	
	P23.3	9	10	P23.2	
RST_S2G2	P23.5	11	12	P23.4	RST_S2G1
	P22.1	13	14	P22.0	
	P21.0	15	16	P22.2	
MDC	P21.2	17	18	P22.3	
	P21.4	19	20	P21.3	MDIO
SPICLK_S2G	P20.10	21	22	P21.5	
TXD_S2G2	P20.0	23	24	P20.1	
RXD_S2G2	P20.3	25	26	/ESR1	ESR1
ESR0	/ESR0	27	28	P20.14	MOSI_S2G
	P15.5	29	30	/PORST	Reset
	P15.4	31	32	P11.12	CLK50
CRS_DV	P11.11	33	34	P11.10	RX_D0
RX_D1	P11.9	35	36	P11.6	TX_EN
TX_D0	P11.3	37	38	P11.2	TX_D1
	VDD_USB	39	40	GND	

Pin Header X2

	GND	1	2	VDD_USB	
	P00.0	3	4	P00.1	
	P00.2	5	6	P00.3	
LED2	P00.6	7	8	P00.5	LED1
	P00.8	9	10	P00.7	Button1
	P00.10	11	12	P00.9	
	P00.12	13	14	P00.11	
	VAREF1	15	16	AN47	
	AN46	17	18	AN45	
	AN44	19	20	AN7	
	AN6	21	22	AN5	
	AN4	23	24	AN3	
	AN2	25	26	AN1	
Potentiometer	AN0	27	28	P33.0	
	P33.1	29	30	P33.2	
	P33.3	31	32	P33.4	
	P33.5	33	34	P33.6	
	P33.7	35	36	P33.8	RXD_S2G1
TXD_S2G1	P33.9	37	38	P33.10	
	+3V3	39	40	GND	

Figure 5 Signal mapping of the pin headers X1 and X2

Note: [1)] Different signal compared with AURIX™ TC275 lite Kit V1.x

4.2 Shield2Go and MikroBus™ Pinout

The pin connectors for the Shield2Go Connectors 1 and 2 and the mikroBus™ can be used to extend the evaluation board or to perform measurements on the AURIX™ TC3X5/TC2X5. Figure 6 shows the available signals at these connectors. The pin table is also printed onto the top and bottom side of the AURIX™ lite Kit V2.

Shield2Go Connector 1

AURIX™ Pins				AURIX™ Pins	
1	+5V	5V			
2	AN16	AN1	RX	P33.8	10
3	AN17	AN2	TX	P33.9	11
4	P13.2[2]	SDA	RST/GPIO2	P23.4[1]	12
5	P13.1[2]	SCL	GPIO1	P32.2	13
6	GND	GND	CS	P20.13[1]	14
7	+3V3	3V3	SCLK	P20.11[1]	15
8	P00.4	INT/GPIO3	MOSI	P20.14[1]	16
9	P14.9[1]	PWM/GPIO4	MISO	P20.12[1]	17

Shield2Go Connector 2

AURIX™ Pins				AURIX™ Pins	
1	+5V	5V			
2	AN18	AN1	RX	P20.3	10
3	AN19	AN2	TX	P20.0	11
4	P13.2[2]	SDA	RST/GPIO2	P23.5[1]	12
5	P13.1[2]	SCL	GPIO1	P32.3	13
6	GND	GND	CS	P20.10[1]	14
7	+3V3	3V3	SLCK	P20.11[1]	15
8	P10.8	INT/GPIO3	MOSI	P20.14[1]	16
9	P14.10[1]	PWM/GPIO4	MISO	P20.12[1]	17

mikroBus™ Connector

1	AN26	AN	PWM	P2.8	16
2	P10.6	RST	INT	P10.7	15
3	P14.7[1]	CS	RX	P15.1	14
4	P15.8[1]	SCK	TX	P15.0	13
5	P15.7[1]	MISO	SCL	P13.1[2]	12
6	P15.6[1]	MOSI	SDA	P13.2[2]	11
7	+3V3	3.3V	5V	+5V	10
8	GND	GND	GND	GND	9

Figure 6 Signal mapping of the pin headers for Mikrobus and Shield2Go Connector 1 and 2

Note: [1] Different signal compared with AURIX™ TC275 lite Kit V1.x

[2] The I2C buses SCL and SDA are shared on the Shield2GOs, mikroBus™, Arduino connectors and the I2C eeprom.

4.3 Arduino Compatible Connector

The mapping of GPIOs and AURIX™ pin functions to Arduino compatible functions can be found in Figure 6. The Arduino compatible connector supports

- SPI interface (SPI_xxx)
- I2C interface (I2C_xxx)
- UART interface (UART_xxx)
- PWM signal outputs (PWM0-13)
- ADC input (ADC0-5)
- Interrupt input (INT0-1)

Note that all pins are cabable of offering more functions than mentioned in Figure 6. For more information about all pin functions, we want to refer you to the corresponding datasheet.

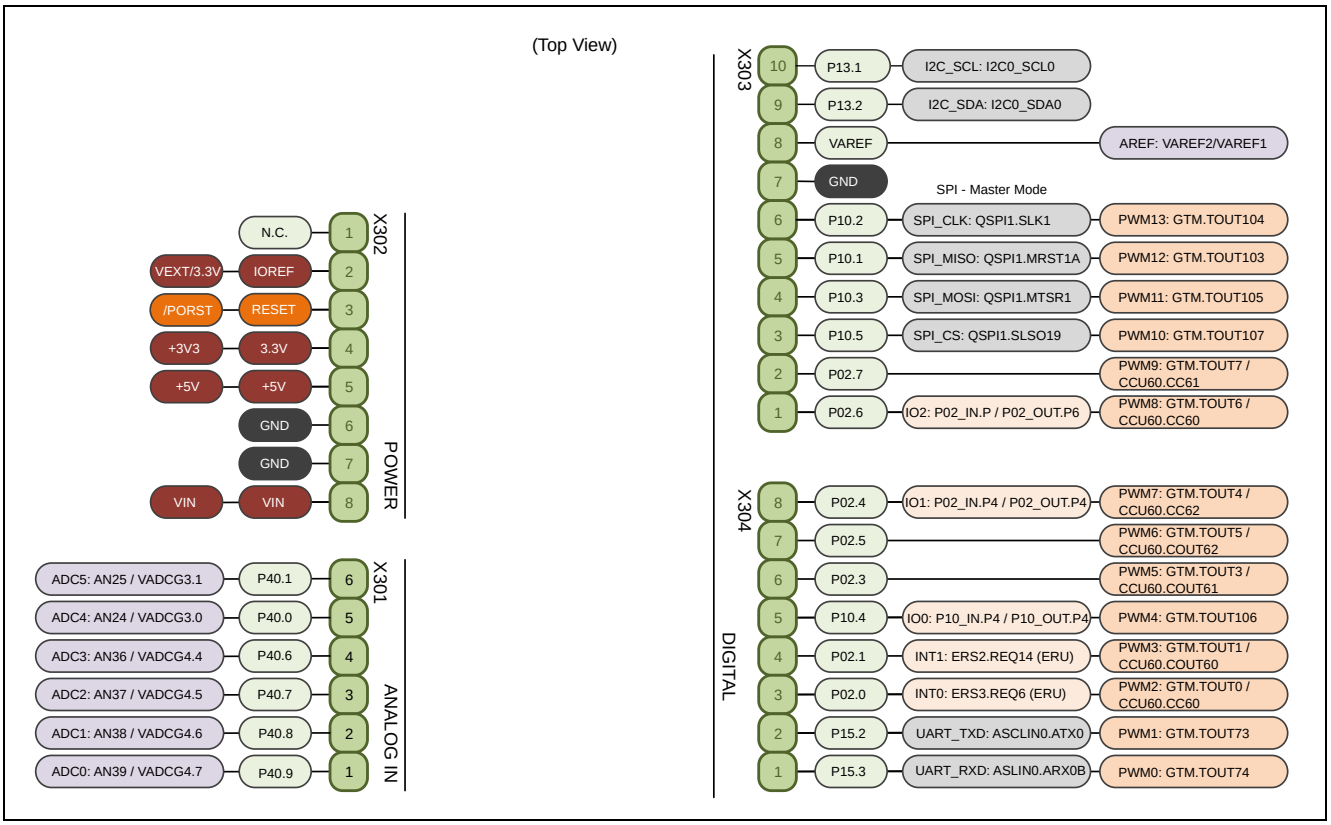


Figure 7 Mapping of Arduino Functions to AURIX™ Pin Functions

The **AURIX™ lite Kit V2** works with 3.3 V logic levels. Therefore, any board that works with 5 V logic levels, cannot be used.

Analog input signals ADC0-5 are limited to a voltage which is smaller or equal than VAREF with VAREF = VDDM = 3.3 V. Primarily, ADC0 to ADC5 should be used as analog input, because there is no additional circuit connected to these pins. Parallel operation of I2C and ADC4 / ADC5 is possible, because they don't share anymore the same pins at the Arduino connector X301 and X303 as on previous AURIX™ lite Kit V1.

4.4 Infineon DAP Debug Connector (10-pin)

Infineon's 10-pin Device Access Port Debug Connector (DAP) is a two-wire tool access port for microcontrollers and similar devices. It allows robust high speed connections over a long cable for automotive applications. The pin assignment of the DAP Debug Connector is shown in Table 9. The board comes with a DAP connector. You can connect a DAP hardware here. If you use this connector make sure that the miniWiggler JDS is not activ (LED5 is off). For more information, we refer you to the DAP Connector Manual.

Table 9 Pin Assignment of the DAP Debug Connector

Pin	Name	AURIX™ Pin	Direction	Description
1	VREF	VEXT	O	Supply voltage from the target system. The voltage has to be strong enough to supply the target side of the level shifters within the tool hardware up to about 20 MHz DAP operating frequency. The required supply current is in the range of 5 mA, mainly caused by signal switching. It can be reduced by lowering frequency and capacitance. Beyond 20 MHz the tool hardware has to supply the level shifter from another source and use this pin just as a voltage reference
2	**DAP1**	TMS	IO	DAP: Data pin.
	SPD		IO	SPD: Data pin.
	UART		IO	Single-wire UART. Serial communication interface (e.g. used for Bootstrap Loader BSL).
3	GND	GND		Recommended pin for signal return of DAP1 for high frequency impedance matching.
4	**DAP0**	TCK	I	DAP: Clock.
	SUP		I	SPD: Optional user pin value for feedback into the target system. Otherwise reserved
5	GND	GND		Recommended pin for signal return of DAP0 for high frequency impedance matching.
6	**DAP2**	P21.7	IO	DAP: Optional second data pin.
	USER0		IO/O	Generic signal that can be used for non specified functions.
7	KEY (GND in cable)	GND	-	If the recommended connector with keying shroud is not used, this pin provides another option to enforce polarization. In that instance this pin is removed from the target connector and the associated jack in the cable connector closed with a plastic pin for example.
8	**DAP3**	/TRST	IO	DAP: Optional third data pin.
	USER1		IO/I	Generic signal that can be used for non-specified functions.
	(DAPEN)		I	Optional indicator that the tool is connected. This can be used to enable the DAP interface of the device
9	GND	GND		Supply ground.
10	RESET	/PORST	IO	Target reset signal. Open drain active low signal. May be used bi-directionally to drive or sense the target reset signal. Usually driven by the tool to reset the target system. The target system is responsible for providing a pull-up to VREF on this signal to establish a logic one. The resistor shall not have a value less than 1 kOhms.

5 Schematics and Placement

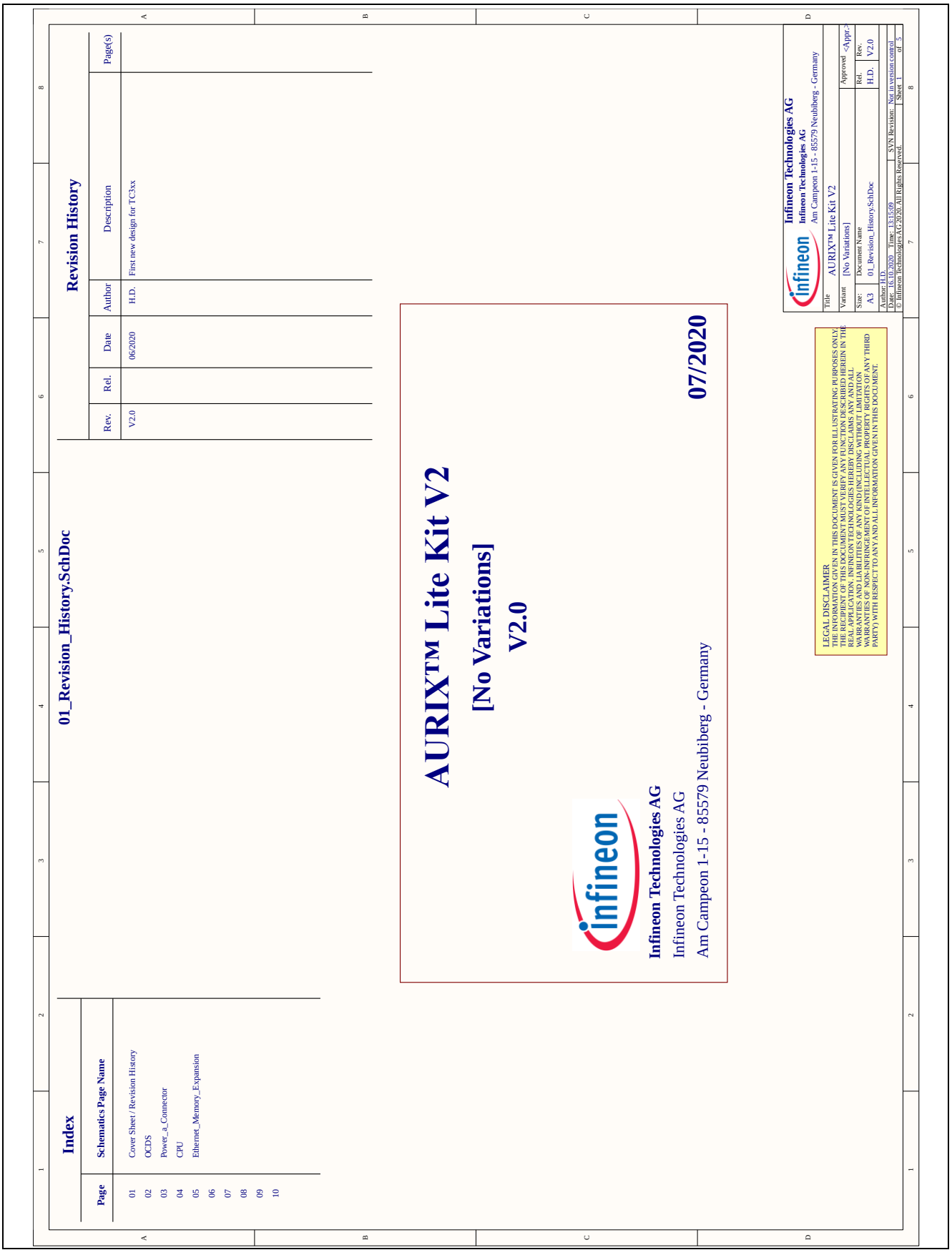


Figure 8 Schematic: Project Overview

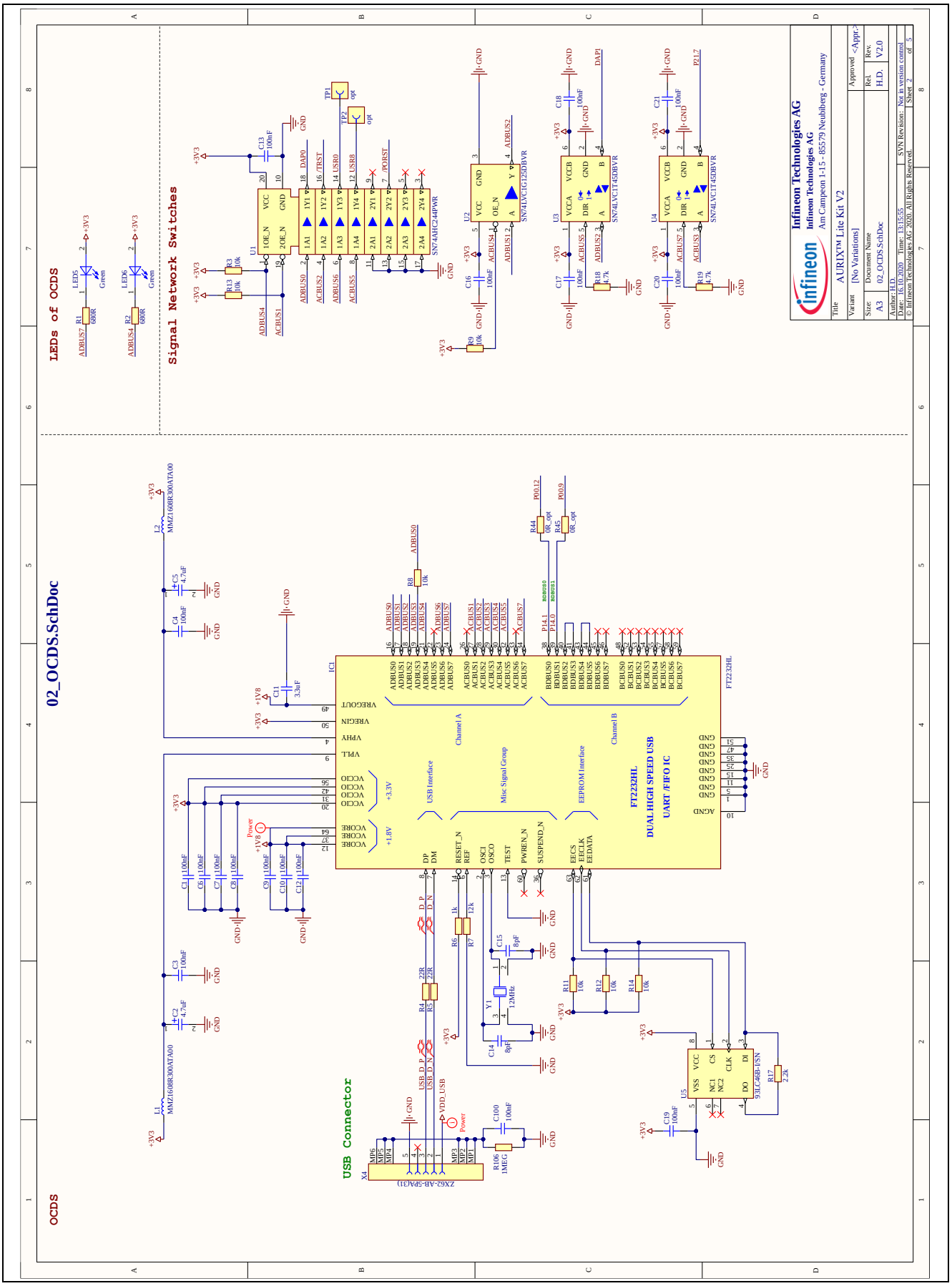


Figure 9 Schematic: On Board miniWiggler

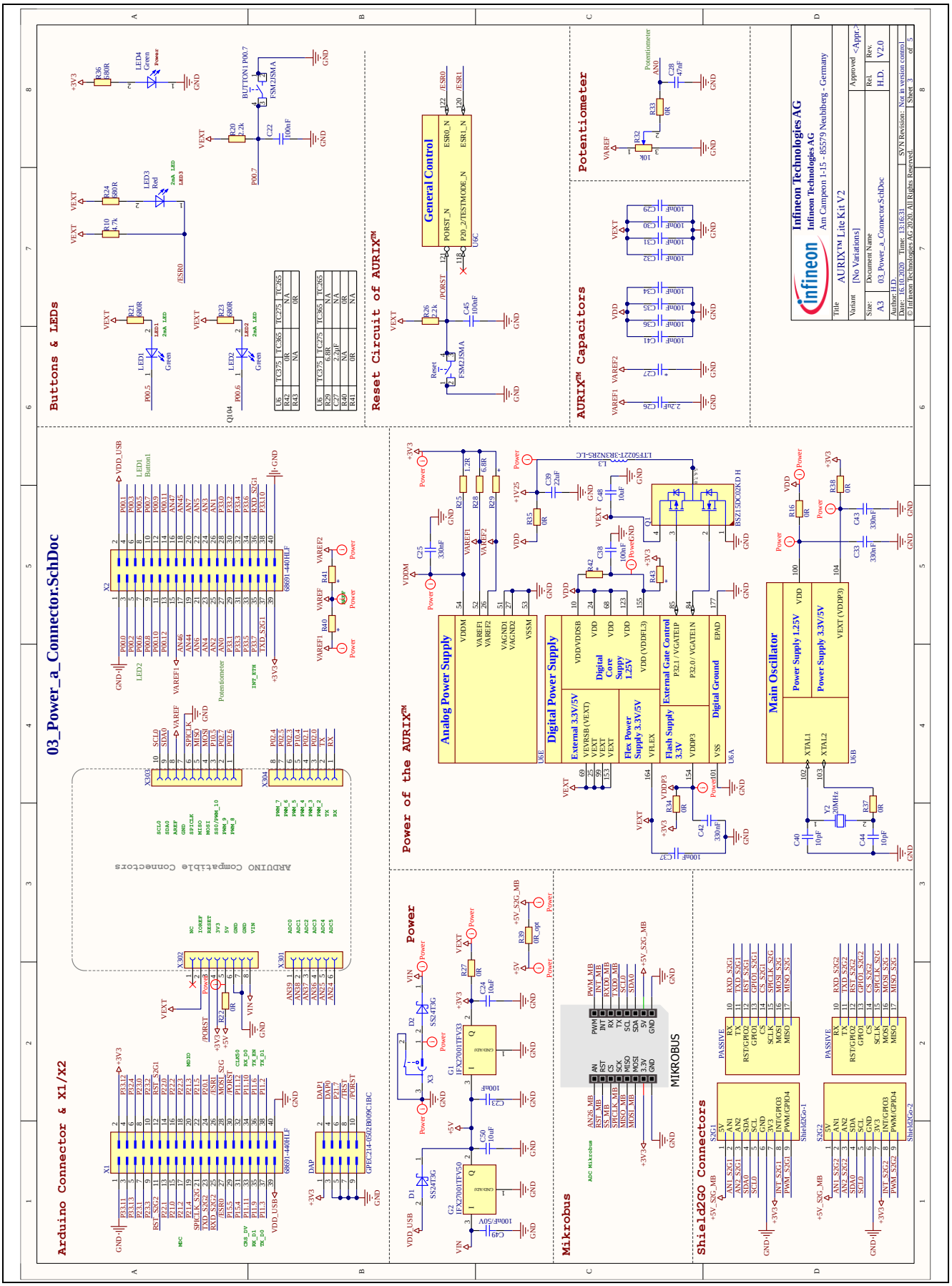


Figure 10 Schematic: Power and Connectors

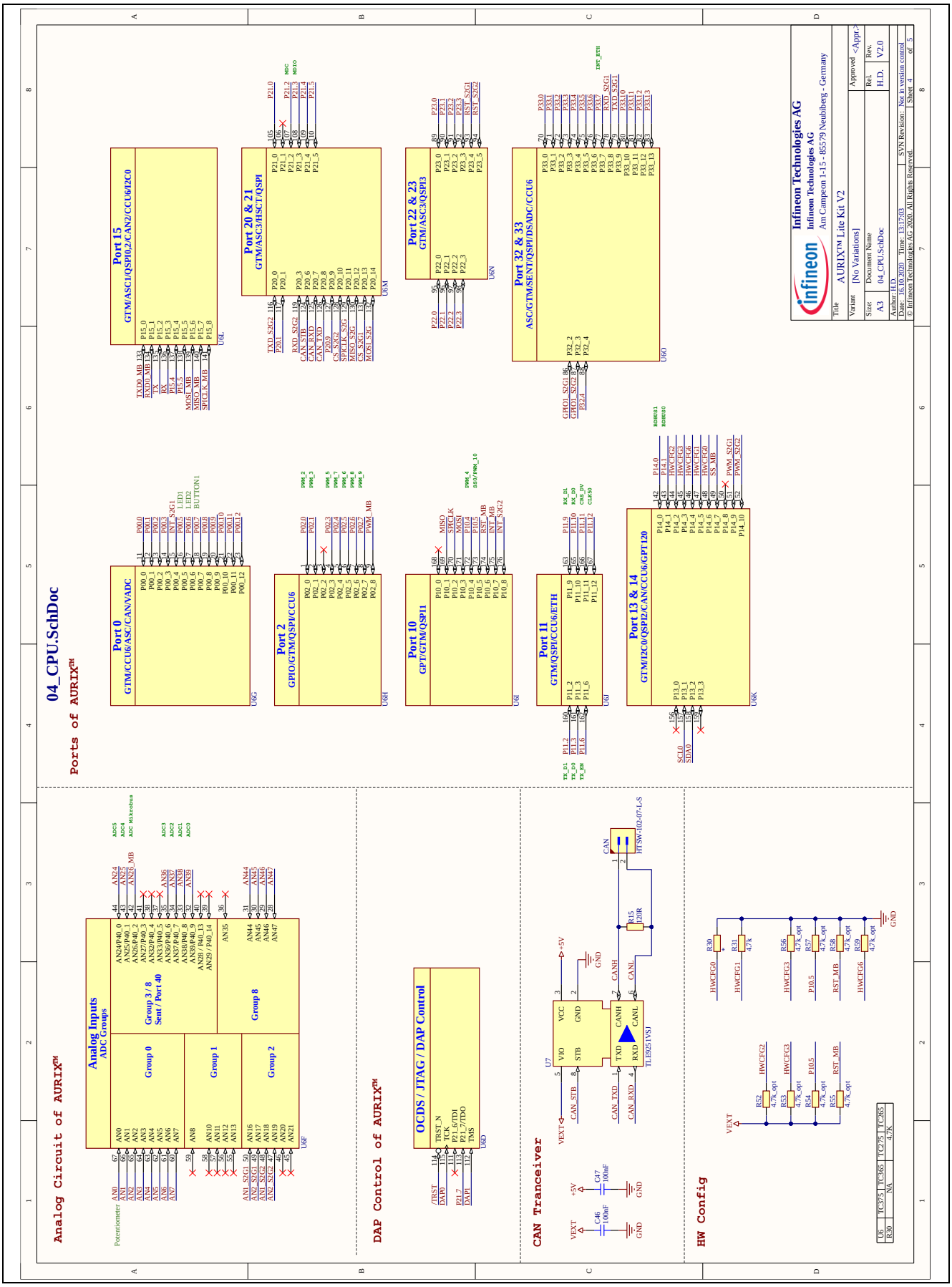


Figure 11 Schematic: CPU and config

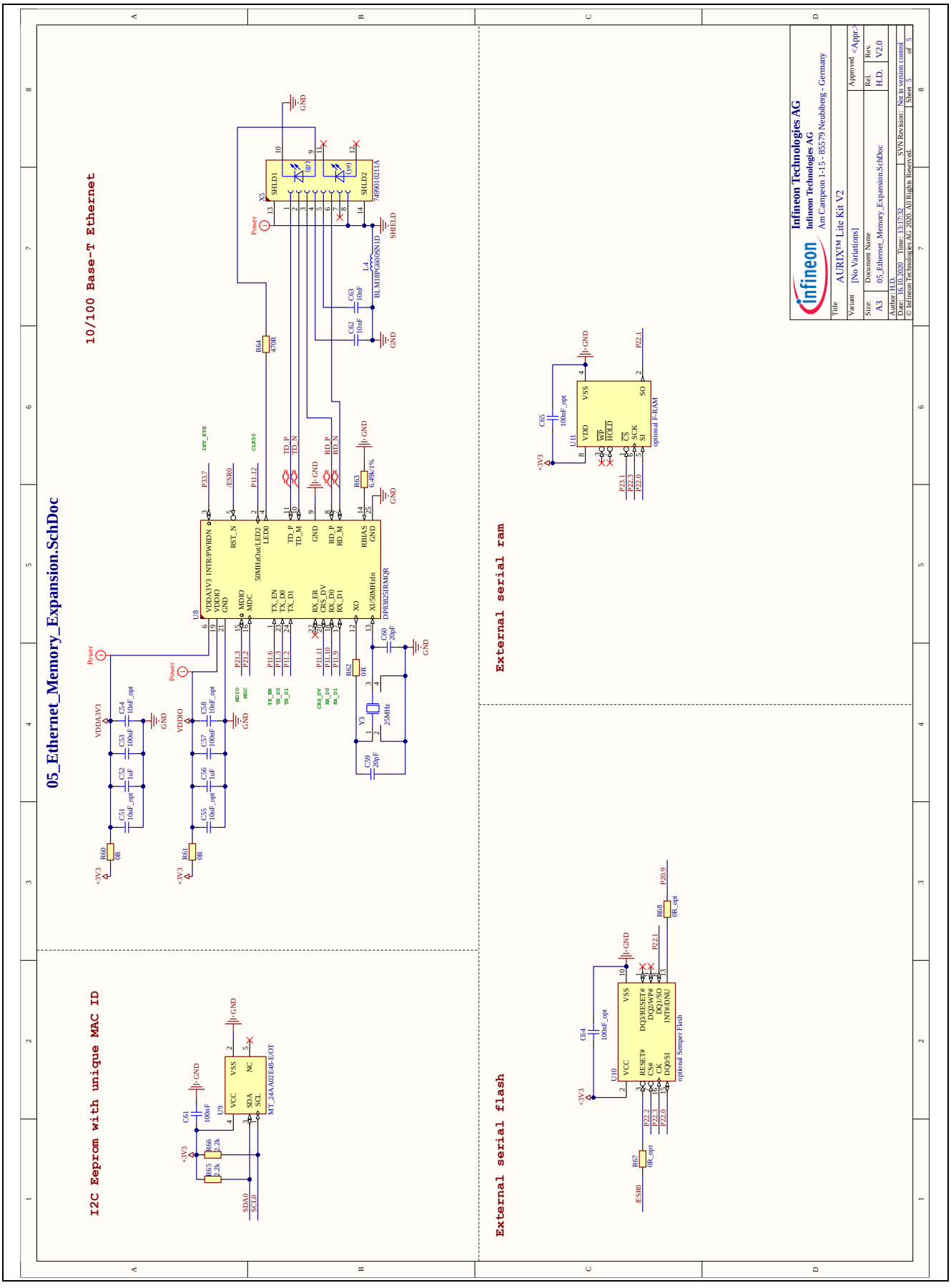


Figure 12 Schematic: Ethernet and memory expansion

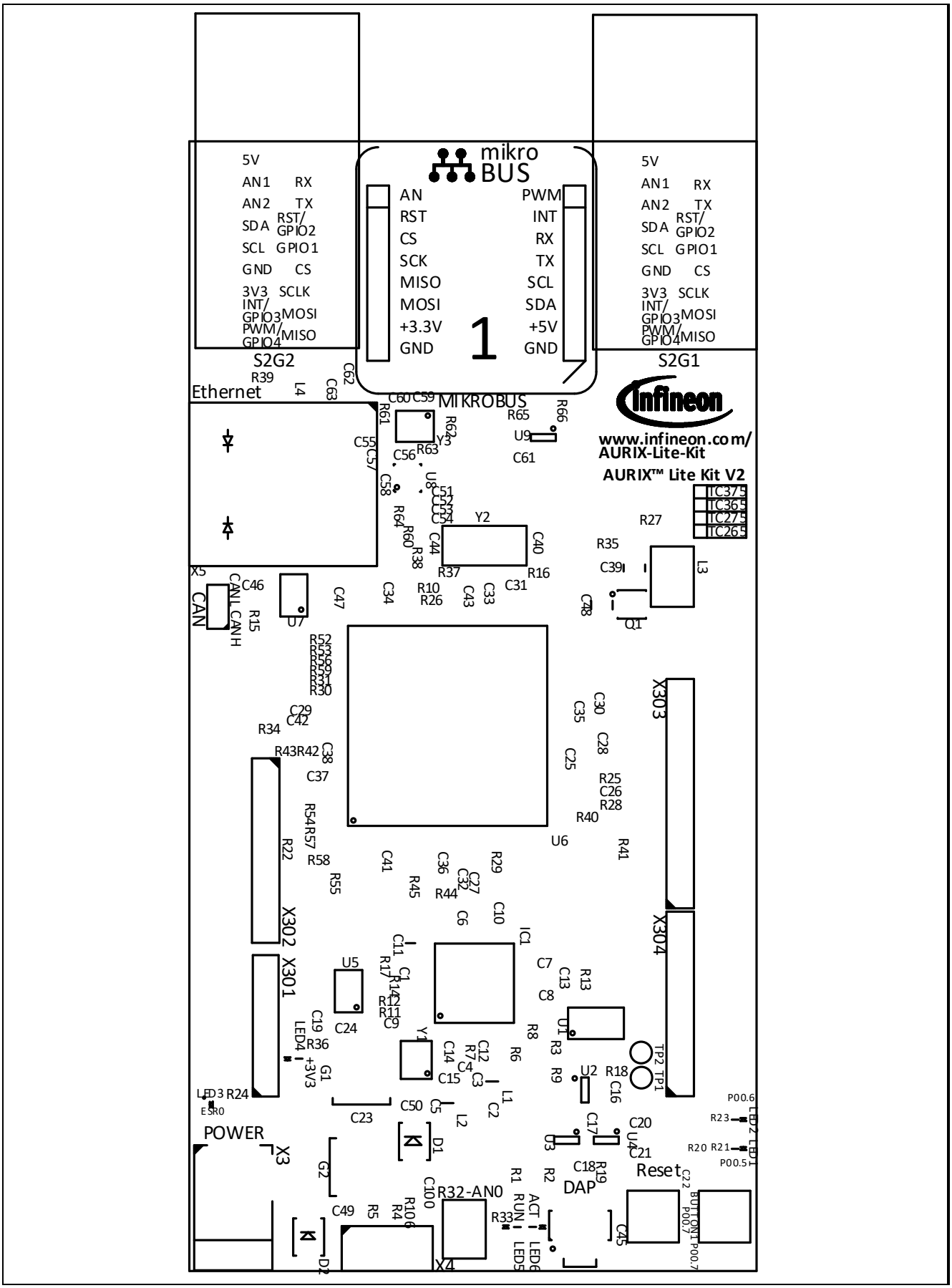
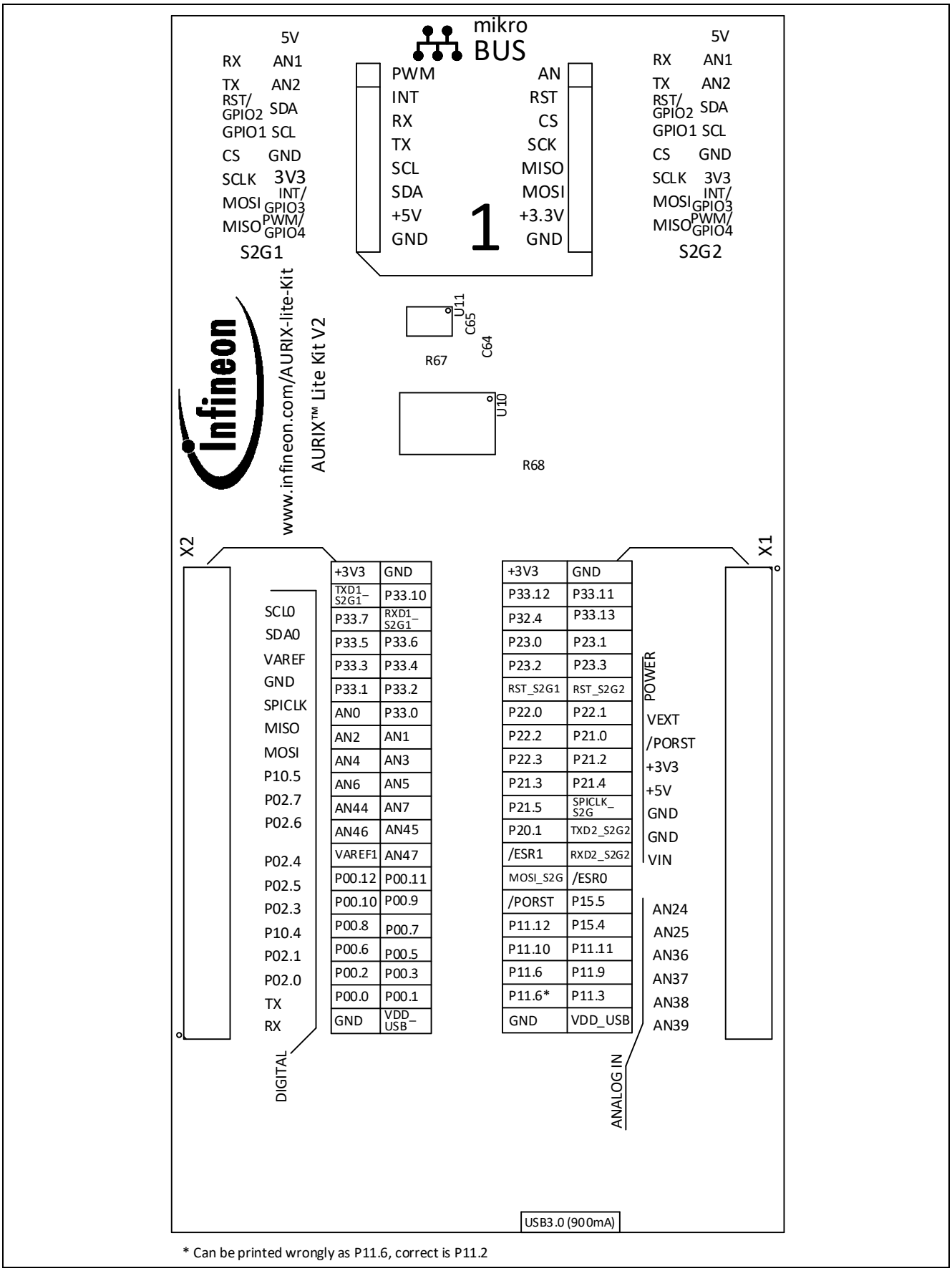


Figure 13 Placement: Top View



* Can be printed wrongly as P11.6, correct is P11.2

Figure 14 Placement: Bottom View

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